Design and Implementation of Multiplexed SPI using FPGA

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***Abstract*- The Serial Peripheral Interface Bus The SPI communication was originally realized for the Fully Configurable Freely Scalable Digital Audio System. First we used Philips's 12C (Inter IC Communication), but it was too slow, and the number of the connected devices was limited. With SPI we can connect as many devices as many pins we have on the main microcontroller. The SPI bus was developed by MOTOROLA Semiconductors. The MAX349/MAX350 are 8-channel and dual 4-channel, serially controlled multiplexer is used for communication in either direction.**

***Keywords*- SPI, FPGA, I2C, SCK, VHDL.**

I. INTRODUCTION

SPI is quite straightforward—it defines features any digital electronic engineer would think of if it were necessary to quickly define a way to communicate between two digital devices. The Serial Peripheral Interface Bus or SPI bus is a synchronous Serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip Select) lines. Sometimes SPI is called a "four wire" serial bus, contrasting with three, two, and one wire serial buses.that operates in full duplex mode. Sometimes SPI is called a "four wire" serial bus.

There is one master and one or more slave devices in the communication. Today, the SPI bus is used in many other application fields than just audio and video equipment. The bus is generally accepted in the industry as a de-facto standard.

Four logic signals are necessary to connect 2 ore more devices with SPI:

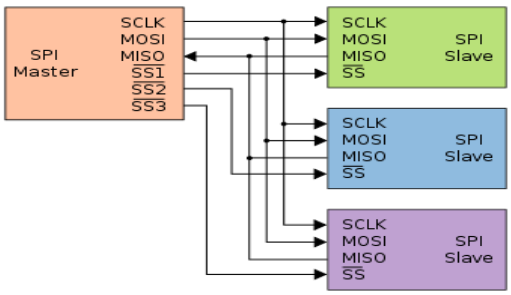


Fig.1: SPI BUS: MASTER AND THREE SLAVES.

Table 1. SPI Interface Pin Descriptions *Note (1)*		
Signal	**Purpose**	**Description**
MOSI	master-out slave-in	Outputs data from the master to the inputs of the slaves.
MISO	master-in slave-out	Inputs data from the master to the outputs of the slaves.
SCLK	master-in slave-out	Transfers data from the slave to the input of the master.
SCLK	SPI clock	Clock driven by the master to the slaves. Used to synchronize the data bits.
SS	slave select	Select signal (active low) is driven by the master and sent to the individual slaves, and is used to select the target slave.

Table 1: SPI interface pin description

a. FEATURES

- Full duplex synchronous serial data transfer
- Variable length of transfer word up to 128 bits
- MSB or LSB first data transfer
- Rx and Tx on both rising or falling edge of serial clock independently
- 8 slave select lines
- Fully static synchronous design with one clock domain
- Technology independent Verilog.
- Technology independent Verilog.
- Fully synthesizable
- As compared with its counterpart I2C, SPI is more suite for data stream applications. Communication between DSPs. ADC
- SPI can also achieve significantly higher data rates than I2C.
- Full Duplex capability.

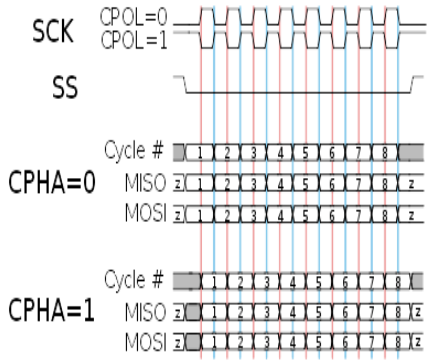
b. CLOCK POLARITY AND PHASE

In addition to setting the clock frequency, the master must also configure the clock polarity and phase with respect to the data. Free scale's SPI Block Guide names these two options as CPOL and CPHA respectively, and most vendors have adopted that convention. The timing diagram is shown to the right. The timing is further described below and applies to both the master and the slave device.

- At CPOL=0 the base value of the clock is zero

- For CPHA=0, data is read on the clock's (low->high transition) and data is changed on a (high->low clock transition).
- For CPHA=1, data is read on the clock's falling edge and data is changed on a rising edge.
- At CPOL=1 the base value of the clock is one (inversion of CPOL=0)
- For CPHA=0, data is read on clock's falling edge and data is changed on a rising edge.
- For CPHA=1, data is read on clock's rising edge and data is changed on a falling edge.

That is, CPHA=0 means sample on the leading (first) clock edge, while CPHA=1 means sample on the trailing (second) clock edge, regardless of whether that clock edge is rising or falling. Note that with CPHA=0, the data must be stable for a half cycle before the first clock cycle. For all CPOL and CPHA modes, the initial clock value must be stable before the chip select line goes active .



c. DATA TRANSMISSION

To begin a communication, the master first configures the clock, using a frequency less than or equal to the maximum frequency the slave device supports. Such frequencies are commonly in the range of 1-70 MHz

The master then pulls the slave select low for the desired chip. If a waiting period is required (such as for analog-to-digital conversion) then the master must wait for at least that period of time before starting to issue clock cycles as shown in figure 2.

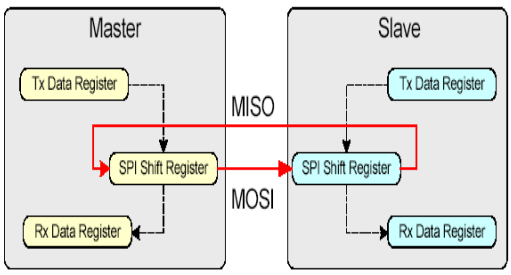
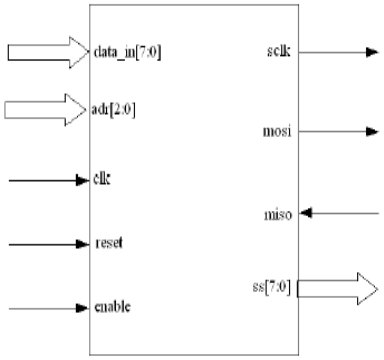


Fig 2: Data Transmission among Master-slave

SPI Master Symbol



d. Pin Description

Pin	Type	Description
data_in[7:0]	input	Data bus input
adr[2:0]	input	Address line
Clk	input	Master clock input
Reset	input	Reset pin
Enable	Input	Enable Pin
Sclk	output	SPI clock output
Mosi	output	Master out-Slave in line

e. Field-programmable gate array: FPGA

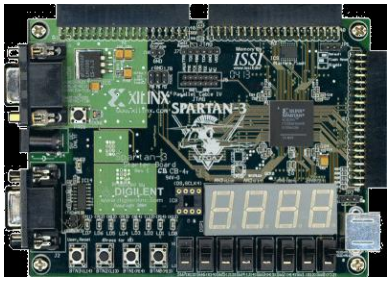
A field-programmable gate array (FPGA) is a semiconductor device that can be configured by the customer or designer after manufacturing—hence the name "field-programmable".

Xilinx Co-Founders, Ross Freeman and Bernard Vonderschmitt, invented the first commercially viable field programmable gate array in 1985 – the XC2064.[3] The XC2064 had programmable gates and programmable interconnects between gates, the beginnings of a new technology and market. The XC2064 boasted a mere 64 configurable logic blocks (CLBs), with two 3-input lookup tables (LUTs).

f. FPGA I HAVE USED

I have used SPARTEN 3 starter kit made by XILINX for my implementation work.

SPARTEN 3 STARTER KIT



Xilinx Spartan-3 FPGA, 200K

Connector(s): Three 40-pin expansion connectors

g. MAX 350 MULTIPLEXER

The MAX349/MAX350 are 8-channel and dual 4-channelserially controlled multiplexers (muxes). These muxes conduct equally well in either direction. On-resistance (100½ max) is matched between switches to 16½ max and is flat (10½ max) over the specified signal range. These CMOS devices can operate continuously with dual power supplies ranging from ±2.7V to ±8V or a single supply between +2.7V and +16V. Each mux can handle rail-to-rail analog signals. The off-leakage current is only 0.1nA at +25°C or 5nA at +85°C.Upon power-up, all switches are off and the internal shift registers are reset to zero.

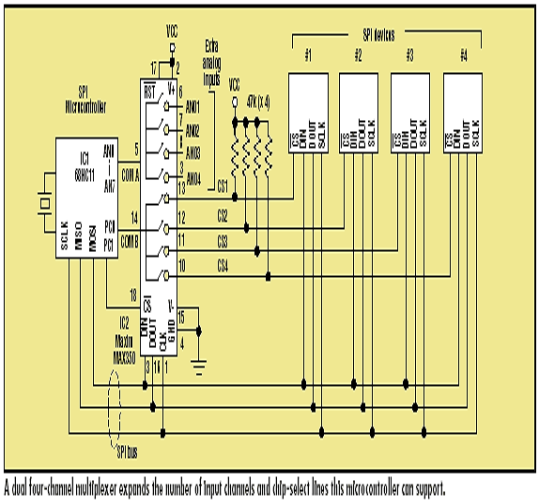
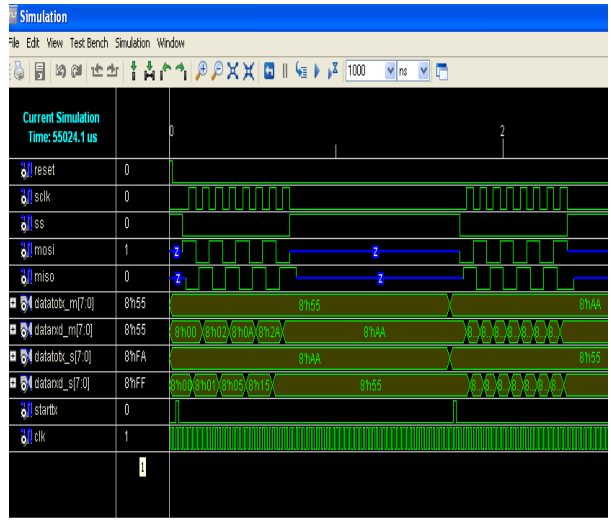
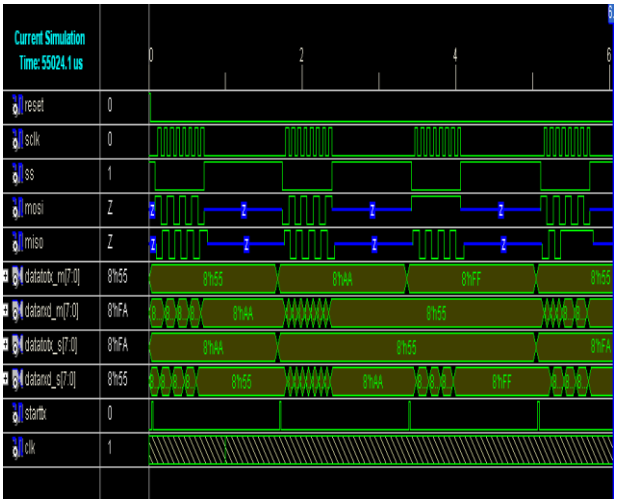


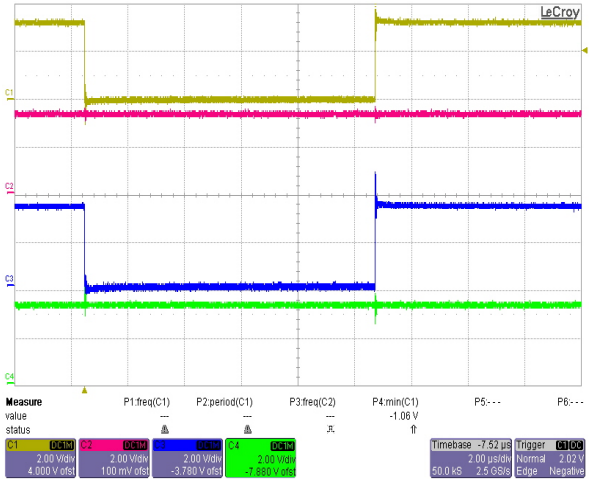
Fig.3 Max 350 Multiplexer

II. SIMULATION RESULTS

During HDL simulation, the simulator software verifies the functionality and timing of the design or portion of the design. The simulator interprets VHDL or Verilog code into circuit functionality and displays logical results of the described HDL to determine correct circuit operation. Simulation allows to create and verify complex functions in a relatively small amount of time. Simulation takes place at several points in the design flow. It is one of the first steps after design entry and one of the last steps after implementation, as part of verifying the end functionality and performance of the design. Simulation is an iterative process, which may require repeating until both design functionality and timing is met.







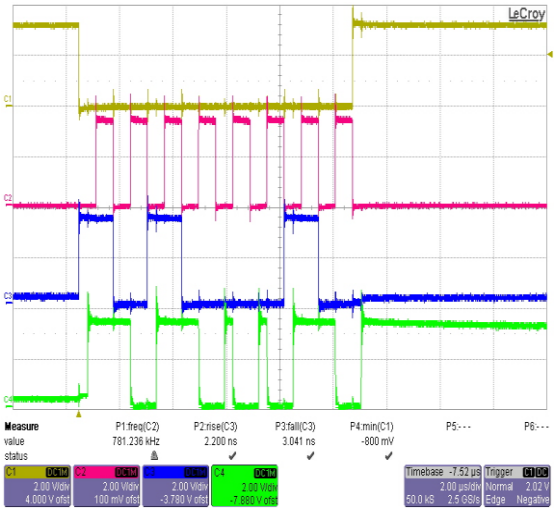


Fig 4:Digital Oscilloscope Results

III. FUTURE SCOPE

- External Slave IC's can b used outside Fpga.
- (7:0),8slaves can be implemented instead of 4.
- Work could be done with High frequency with the availability of requirement.
- High speed or else Multiplexer with latest SPI support can be used.
- Different Board of FPGA can be taken for Implementation.
- Work can be proposed over clock frequency more than 50 MHz with the availability of hardware as per requirement.

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