GENERALIZED PWM ALGORITHM FOR THREE PHASE n-LEVEL VOLTAGE SOURCE INVERTER FED AC DRIVES

M. Khaimulla[1] G.Srinivasa Rao[2] D.Nagaraju[3] and P Shashavali[4]

***Abstract*— This paper presents space vector based pulse width modulation (SVPWM) algorithm for voltage source inverters fed AC drives by using the concept of offset time. To reduce the harmonic distortion and to increase the dc bus utilization of the inverter when compared with the sinusoidal PWM (SPWM) algorithm, this paper has been focused on the implementation of space vector based PWM algorithm. The proposed PWM algorithm have been developed by using the instantaneous phase voltages and hence reduce the complexity involved in the conventional space vector approach. Moreover the proposed algorithm can be easily extended to multilevel inverters. To validate the proposed algorithm, numerical simulation studies and THD analysis has been carried out on v/f controlled induction motor drive and results are presented.**

***Index Terms* — PWM, SVPWM, Multilevel inverters, THD, Induction motor drive.**

I. INTRODUCTION

Due to the inventions of fast switching power semiconductor devices and motor control algorithms, a growing interest is found in a more precise pulse width modulation (PWM) method. During the past decades several PWM algorithms have been studied extensively. Various PWM methods have been developed to achieve wide linear modulation range, less switching loss, less total harmonic distortion (THD) and easy implementation and less computation time. A large variety of algorithms for PWM exist, and a survey of these was given in [1]. There are two popular approaches for the implementation of PWM algorithms, namely triangular comparison (TC) approach and space vector (SV) approach. For a long period, TC approach based PWM methods were widely used in most applications. The earliest modulation signals for TC approach based PWM are sinusoidal. But, the addition of the zero sequence signals to the sinusoidal signals results in several non-sinusoidal signals. Compared with sinusoidal PWM (SPWM) algorithm, non-sinusoidal PWM algorithms can extend the linear modulation range for line-to-line voltages. Different zero-sequence signals lead to different non sinusoidal PWM modulators [2].

Nowadays, due to the development of digital signal processors, SVPWM has become one of the most popular PWM methods for three-phase inverters [3]-[4]. It uses the SV approach to compute the duty cycle of the switches. The main features of this PWM algorithm are easy digital implementation and wide linear modulation range for output line-to-line voltages. The equivalence between TC and SV approaches has studied in [5] and concluded that SV approach offers more degrees of freedom compared to TC approach.

However, the conventional space vector approach requires angle and sector information and hence increases the complexity involved in the algorithm. to reduce the complexity involved, simplified approaches have been proposed in [6]-[8] by using the concept of imaginary switching times and offset time.

In this paper, space vector based PWM algorithm for AC drives are presented by using the concept of offset time. Furthermore, the simulation of the proposed PWM method is discussed and simulation results are provided to validate the drawn conclusions.

II. CONVENTIONAL SVPWM ALGORITHM

The main purpose of the voltage source inverter (VSI) is to generate a three-phase voltage with controllable amplitude, and frequency. A general 2-level, 3-phase VSI feeding a three-phase induction motor is shown in Fig 1.

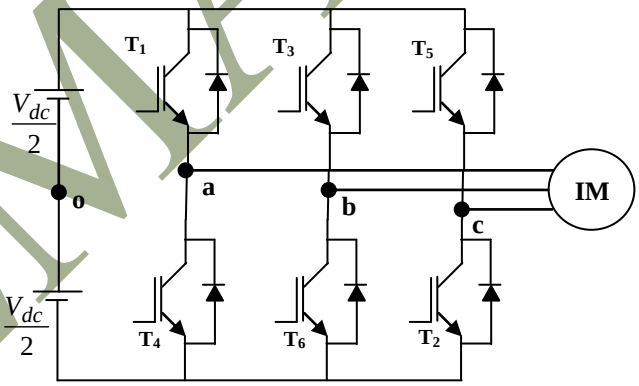


Fig. 1 2-level, 3-phase voltage source inverter feeding induction motor

From Fig. 1, it can be observed that the two switching devices on the same leg cannot be turned on and cannot be turned off at the same time, which will result in the uncertain voltage to the connected phase. Thus the nature of the two switches on the same leg is complementary. The switching-on and switching-off sequences of a switching device are represented by an existence function, which has a value of unity when it is turned on and becomes zero when it is turned off. The existence function of a VSI comprising of switching devices T_i is represented by S_i, i = 1, 2, . . . , 6. Hence, S_1, S_4 which take values of zero or unity respectively, are the existence functions of the top device (T_1) and bottom device (T_4) of the inverter leg which is connected to phase 'a'.

$$S_1 + S_4 = 1;\ S_3 + S_6 = 1;\ S_5 + S_2 = 1 \qquad (1)$$

As seen from Fig 1, there are totally six switching devices and only three of them are independent. The combination of these three switching states gives out eight possible voltage vectors. At any time, the inverter has to operate one of these voltage vectors. Out of eight voltage vectors, two are zero voltage vectors (V_0 and V_7) and remaining six (V_1 to V_6) are active voltage vectors. In the space vector plane, all the voltage vectors can be represented as shown in Fig 2.

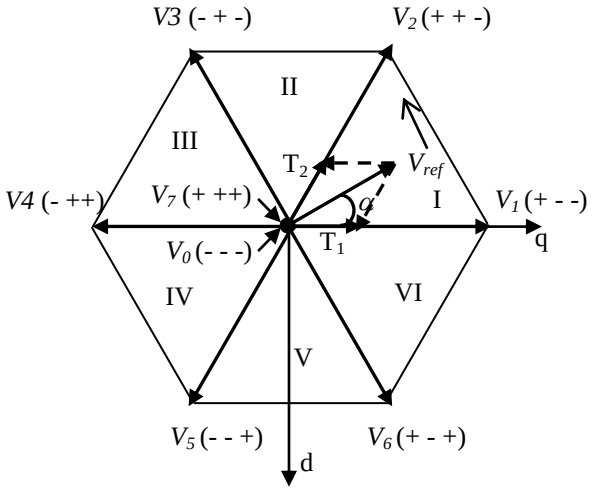


Fig. 2 Voltage space vectors produced by a voltage source inverter

For a given set of inverter phase voltages (V_{an}, V_{bn}, V_{cn}), the space vector can be constructed as

$$V_s = \frac{2}{3}\left(V_{an} + V_{bn}e^{j\frac{2\pi}{3}} + V_{cn}e^{j\frac{4\pi}{3}} \right) \quad (2)$$

From (2), it is easily shown that the active voltage vectors or active states can be represented as

$$V_k = \frac{2}{3}V_{dc}e^{j(k-1)\frac{\pi}{3}} \qquad \text{where } k = 1,2,\ldots,6 \quad (3)$$

By maintaining the volt-second balance, a combination of switching states can be utilized to generate a given sample in an average sense during a subcycle. The voltage vector V_{ref} in Fig.2 represents the reference voltage space vector or sample, corresponding to the desired value of the fundamental components for the output phase voltages. But, there is no direct way to generate the sample and hence the sample can be reproduced in the average sense. The reference vector is sampled at equal intervals of time, T_s referred to as sampling time period. Different voltage vectors that can be produced by the inverter are applied over different durations with in a sampling time period such that the average vector produced over the subcycle is equal to the sampled value of the reference vector, both in terms of magnitude and angle. As all the six sectors are symmetrical, here the discussion is limited to sector-I only. Let T_1 and T_2 be the durations for which the active states 1 and 2 are to be applied respectively in a given sampling time period T_s. Let T_z be the total duration for which the zero states are to be applied. From the principle of volt-time balance T_1, T_2 and T_z can be calculated as:

$$T_1 = \frac{2\sqrt{3}}{\pi} M \left[Sin(60^o - \alpha) \right] T_s \quad (4)$$

$$T_2 = \frac{2\sqrt{3}}{\pi} M \left[Sin(\alpha) \right] T_s \quad (5)$$

$$T_Z = T_s - T_1 - T_2 \quad (6)$$

where M is known as the modulation index and defined as given in (7).

$$M = \frac{\pi v_{\text{ref}}}{V_{dc}} \quad (7)$$

In the SVPWM algorithm, the maximum modulation index is 0.906 [1]. In the SVPWM strategy, the total zero voltage vector time is equally distributed between V_0 and V_7. Further, in this method, the zero voltage vector time is distributed symmetrically at the start and end of the subcycle in a symmetrical manner. Moreover, to minimize the switching frequency of the inverter, it is desirable that switching should take place in one phase of the inverter only for a transition from one state to another. Thus, SVPWM uses 0127-7210 in first sector, 0327-7230 in second sector and so on. Table-1 depicts the switching sequence for all the sectors.

TABLE I
SWITCHING SEQUENCES IN ALL SECTORS FOR SVPWM

Sector number	On-sequence	Off-sequence
1	0-1-2-7	7-2-1-0
2	0-3-2-7	7-2-3-0
3	0-3-4-7	7-4-3-0
4	0-5-4-7	7-4-5-0
5	0-5-6-7	7-6-5-0
6	0-1-6-7	7-6-1-0

Also, with the SVPWM algorithm, the modulation index and dc bus utilization can be increased when compared with the SPWM algorithm [1].

III. PROPOSED PWM ALGORITHM

To reduce the complexity involved in the existing SVPWM algorithm, in this section, the proposed PWM algorithms have been developed by using the notion of imaginary switching times. In this approach, the imaginary switching time periods proportional to the instantaneous values of the reference phase voltages are calculated as given in (8) [6]-[7].

$$\begin{aligned} T_{an} &\equiv \left(\frac{T_s}{V_{dc}} \right) V_{an} \\ T_{bn} &\equiv \left(\frac{T_s}{V_{dc}} \right) V_{bn} \\ T_{cn} &\equiv \left(\frac{T_s}{V_{dc}} \right) V_{cn} \end{aligned} \quad (8)$$

To calculate the active vector switching times, the maximum, middle and minimum values of imaginary switching times are calculated in every sampling time as given in (9) – (11).

$$T_{\max} = Max(T_{an}, T_{bn}, T_{cn}) \quad (9)$$

$$T_{mid} = Mid(T_{an}, T_{bn}, T_{cn}) \quad (10)$$

$$T_{\min} = Min(T_{an}, T_{bn}, T_{cn}) \quad (11)$$

Then, the effective time during which the induction motor is effectively connected to the source (that is the power will be transferred to the motor from source) can be calculated as given in (12).

$$T_{eff} = T_{\max} - T_{\min} \quad (12)$$

When the actual gating signals for power devices are generated in the PWM algorithm, there is one degree of freedom by which the effective time can be relocated anywhere within the sampling time period. Therefore, the actual switching times for each inverter leg can be obtained by the time shifting operation as follows:

$$T_{ga} = T_{an} + T_{offset} \quad (13)$$

$$T_{gb} = T_{bn} + T_{offset} \quad (14)$$

$$T_{gc} = T_{cn} + T_{offset} \quad (15)$$

where

$$T_{offset} = T_s(1-\mu) + (\mu - 1)T_{\max} - \mu T_{\min} \quad (16)$$

To guarantee the full utilization of dc-link voltage of the inverter, the actual switching times should be restricted to a value from 0 to T_s.

In the implementation of the proposed offset time based unified PWM algorithm, the zero voltage vector time partition parameter (μ) can take any form (constant or time-varying) ranging between 0 and 1. The choice of μ affects the average neutral voltage. In the conventional SVPWM algorithm, as the zero voltage vector time is distributed equally, μ is generally taken as 0.5. If μ is either 0 or 1, each switching device ceases to switch for a total of 120 degrees per fundamental cycle. Hence, the switching losses and effective inverter switching frequency are significantly reduced. As the modulating signals are discontinuous, these PWM algorithms are also known as DPWM algorithms or bus-clamping PWM algorithms.

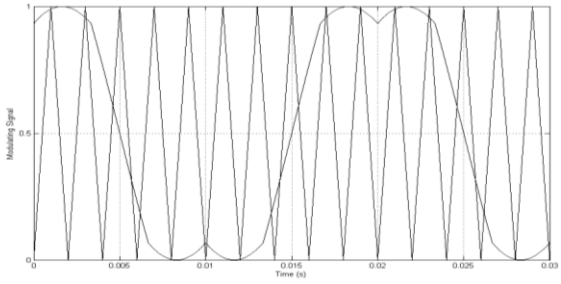
The SVPWM, DPWMMIN and DPWMMAX algorithms can be obtained for μ = 0.5, 1 and 0 respectively.

IV. EXTENSION TO MULTILEVEL INVERTERS

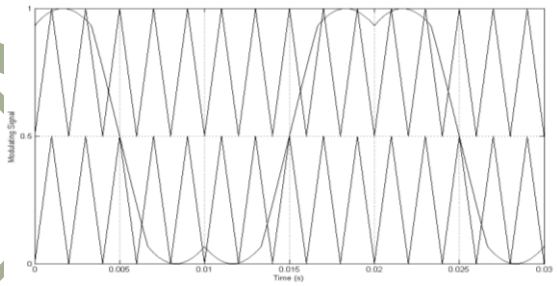
The recent industrial applications require high power apparatus. The classical Two-level inverters may not be useful in high voltage range (above 2 kV) due to limited rating of switches. In conventional two-level inverter configurations, the harmonic contents reduction of an inverter output current is achieved mainly by increasing the switching frequency. But the switching frequency is restricted by the switching losses in high power and high voltage applications [9]. In such applications, multilevel inverters have been widely used in recent years for the advantage of low harmonic output at low switching frequency. At the same time, low blocking voltage in the switching devices can be achieved. As a result, multilevel power inverter structure has been introduced as an alternative in high power and medium voltage situations [10].

The multilevel inverters have several advantages like i) Staircase waveform quality*:* Multilevel inverters can generate the output voltages with very less distortion. As level of inverter increases, the output voltage is nearer to sinusoidal. ii) Voltage stress reduction*:* Multilevel inverter can reduce voltage stress on switching devices. iii) Input current quality*:* Multilevel inverters can draw input current with less distortion. iv) Reduction in Total Harmonic Distortion (THD): Multilevel inverter output can have less harmonic content compared to two level waveforms operating at the same switching frequency [11].

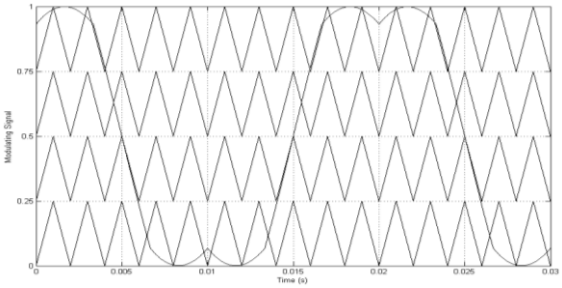
The proposed approach can be easily extended with few variations to the control of multilevel inverters. With reference to the generation of control signals, in this case, the main idea is to manage each voltage level independently from the other levels. Considering multicarrier and a single reference is equivalent to considering only one carrier and more reference voltages [12]. Carrier based modulation techniques control each phase leg of an inverter separately and allow the line to line voltage to be developed implicitly. The multilevel carrier based SVPWM for N-level inverter uses a set of N-1 adjacent level triangular carrier waves with the same peak-to-peak amplitude and the same frequency [13] as shown in fig 3((a),(b),(c)).



a) Modulating Wave and Carrier Wave comparison for two level VSI



b) Modulating Wave and Carrier Wave comparison for three level VSI



c) Modulating Wave and Carrier Wave comparison for five level VSI

Fig. 3 Modulating Wave and Carrier Wave comparison for VSI

V. SIMULATION RESULTS AND DISCUSSIONS

To validate the proposed PWM algorithm, several numerical simulation studies have been carried out on v/f controlled induction motor drive using Matlab-Simulink. For the simulation studies, the average switching frequency of the inverter is taken as 5 kHz, fundamental frequency is taken as 50Hz and the dc link voltage is taken as 600 V. Modulating Wave and Multicarrier Wave comparison for two level, three level and five level are shown in fig 3(a),(b),(c). Modulating waveforms, pole voltages, phase voltages, line voltages and steady state stator current wave of two level, three level and five level inverters are shown in fig (4)-(6). Moreover, the

harmonic distortions of line voltage and steady state current along with the total harmonic distortion (THD) values are given in fig (7)-(12). From the simulation results it can be observed that the proposed approach gives same results when compared with the existing approaches. The THD values of line to line voltages are highly reduced as level increases. The input current drawn by the induction motor is less distorted as level of inverter increases. Moreover as the number of levels increases the output voltage has more steps and nearer to sinusoidal with less distortion. This allows mitigation of the harmonics at low switching frequencies thereby reducing switching losses.

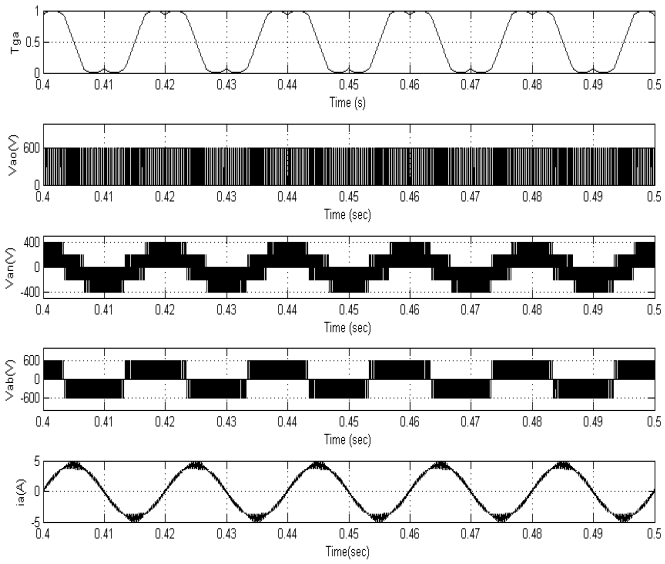


Fig 4 Simulation results of Proposed SVPWM for two level VSI

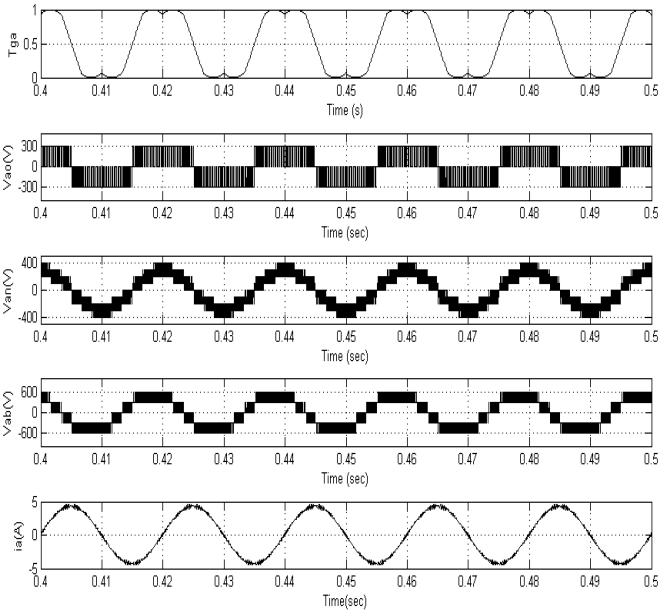


Fig 5 Simulation results of Proposed SVPWM algorithm for three level VSI

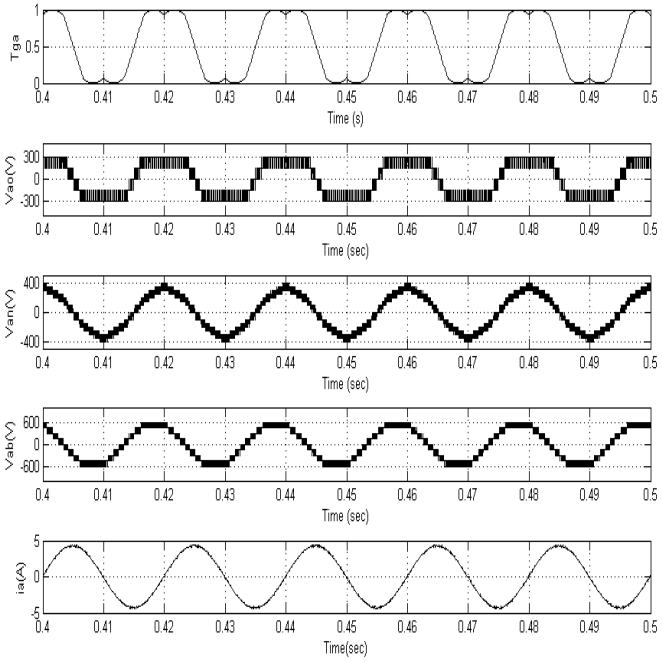


Fig 6 Simulation results of Proposed SVPWM algorithm for five level VSI

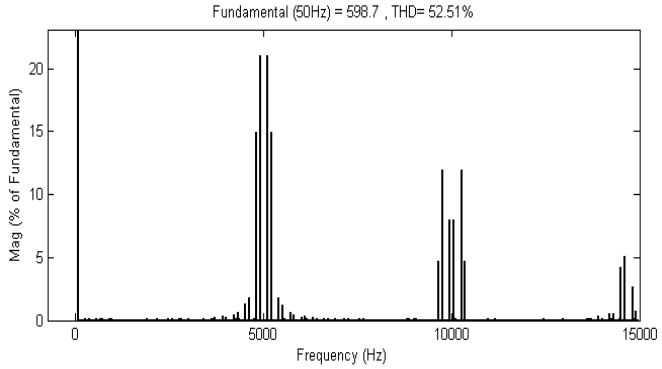


Fig. 7 Harmonic spectra of line voltage for two level inverter at f=50 Hz

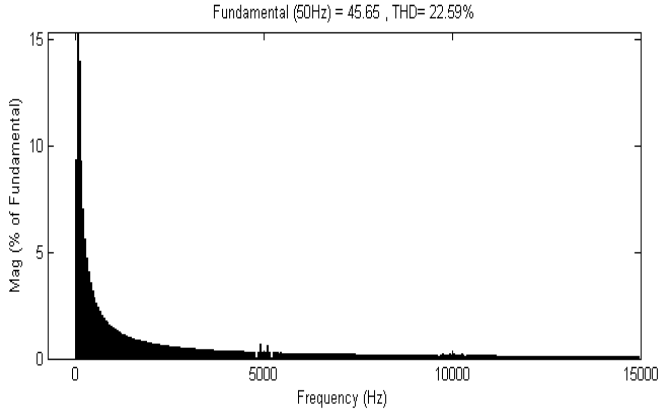


Fig. 8 Harmonic spectra of stator current for two level inverter at f=50 Hz

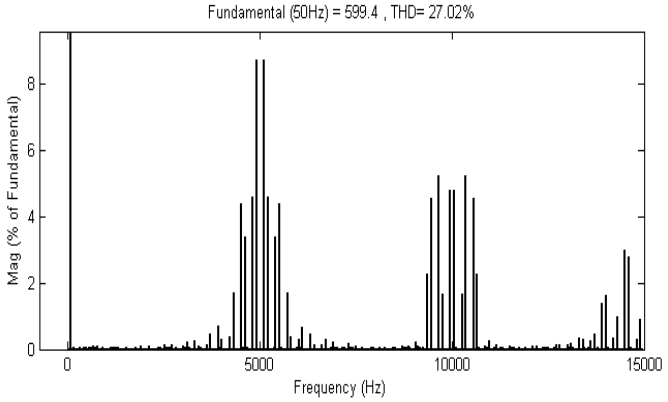


Fig. 9 Harmonic spectra of line voltage for three level inverter at f=50 Hz

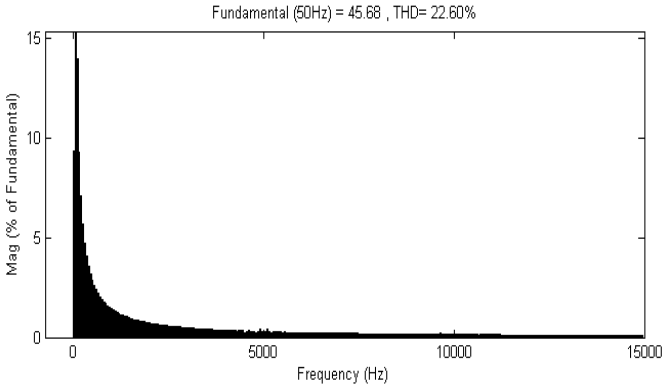


Fig. 10 Harmonic spectra of stator current for three level inverter at f=50 Hz

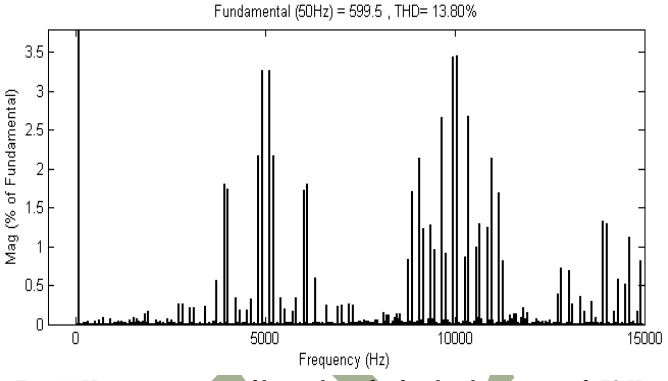


Fig. 11 Harmonic spectra of line voltage for five level inverter at f=50 Hz

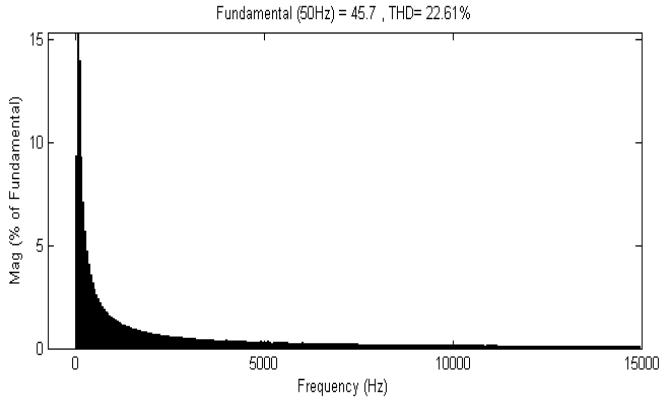


Fig. 12 Harmonic spectra of stator current for five level inverter at f=50 Hz

VI. CONCLUSION

A simple proposed SVPWM algorithm has been developed and simulation results are presented in this paper. The proposed algorithm uses a generalized expression for offset time and by varying which various PWM algorithms are generated. Moreover, the proposed algorithm uses only reference phase voltages and eliminates the angle and sector calculations. The proposed algorithm can be easily extended to multilevel inverters simply by comparing the modulating wave and multicarrier wave. For a N-level inverter N-1 carrier waves with the same peak-to-peak amplitude and the same frequency are required. Simulation results for two level, three level and five level inverters are presented. THD analysis of line to line voltages and steady state stator current are also presented. From the simulation results it can be observed that the THD values of line to line voltages are highly reduced and the input current drawn by the motor is less distorted as level increases. Moreover the output voltage is a staircase and nearer to sinusoidal with less distortion as the level increases.

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