Power Estimation for the 64 -bit RISC Based Processor: As performance Measure

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Abstract-
The power estimation for a processor is key task in the design based on RISC architecture. In this paper we have proposed, power estimation of 64-bit RISC as performance measure with processor with the help of BIST (built in self test) parameters design using VHDL. The results are analyzed using Xilinx ISE and IUS with features of depiction the 64-bit RISC processor with accepted MIPS Architecture, instruction data path, modules of decoder, instruction set, pipelining Architecture are analyzed. Implementation of design

Keywords: Power Estimation, FPGA Design, RISC, ALU, BIST.

I. INTRODUCTION:

Reducing the power consumption of a processor is typical task for developer, which can enhance performance capacity of FPGA devices. The increasing complexity demands design approaches, which can grapple with designs containing hundreds of thousands of memories, logic gates, high-speed interfaces, and other high-enforcement components. One of category such design approaches is delineation methodologies based on language VHDL [1]. It allows designers to develop hardware systems at high level [2]. RISC or Reduced Instruction Set Computer is design philosophies that become main stream in the last few years, as the quest for raw speed has dominated the highly competitive computer industry. There is a desire to enhance the processor's speed and simplify the hardware for reasons of cost. RISC design resulted in computers that execute instructions faster than other computers put together of the same technology [3]. In a RISC machine, the instruction set is based upon a load/store avenue. Only load and store instructions access memory. No I/O or arithmetic, logic instruction operates directly on memory contents. This is a key to single-cycle instructions execution .The simplification results in an instruction decoder that is small, fast and relatively easy to design [3]. Due to the prosperous performance, simple instruction formats, breadth of products and depth of support, the MIPS RISC processor architecture becomes the market eminence in high level performance embedded 32-bit and 64-bit RISC processors [1, 4]. The application of VHDL for modeling is especially appealing since it provides a formal description of the system design and allows the use of specific description styles to disguise the different abstraction levels (register transfer, architectural, and logic level) employed in the design [5, 6, 7] The synthesis helps to integrate the design Work and provides a higher expediency to analyze a far wider range of architectural alternative [7, 8, 9].

II. THE MICRO RISC ARCHITECTURE:

Processors consist of two main parts, the arithmetic/logic unit and the control unit. The arithmetic and logical operations perform by former; the latter controls the flow of operations. In addition to the processor there is memory. A RISC can consists of a memory who's distinctively

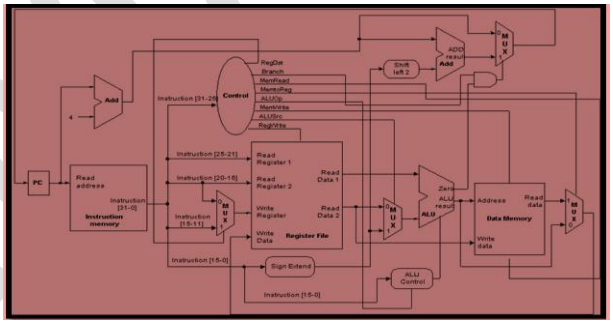

Fig. 1 (a) RISC Processor Architecture

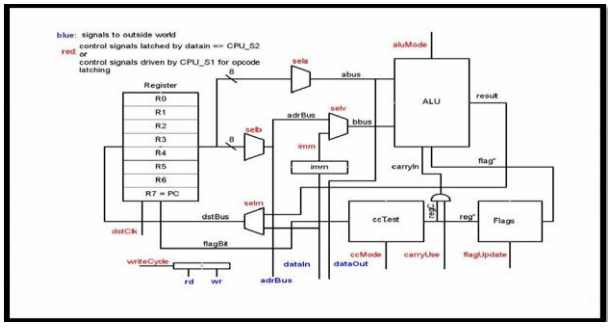

Fig.1(b)Data path diag. for 64-bit RISC Processor

Addressable elements are bytes (8 bits). The ALU features a bank of 16 registers with 64 bits. 64-bit quantities are called words. A characteristic is that every instruction takes one clock cycle for its execution, perhaps with the exception of access to creeping memory. This cycle rule makes such processors predictable in performance. The number of cycles and the time required for executing any instruction sequence is precisely defined. Predictability is essential in all real-time applications.

III. REDUCTION TECHNIQUES OF POWER:

The concern of the power consumption based in any microprocessor system that is Power dissipation is either dynamic or static. Static power dissipation is caused due to the leakage and short circuit current while dynamic power dissipation is due to switching activity of the various transistors in the circuit. A dynamic power forms the major gob of power dissipation in CMOS circuits and has required a lot of attention. In this design power reduction is achieved through bypassing pipeline stages that cause unnecessary switching activity. The influence factors of dynamic power dissipation is switching activity and dynamic power is given by the equation,

P = 0.5*C* (Vdd)*2E (sw)*Fclk to decreasing switching activity (E (sw)) results in reduced dynamic power consumption.

Tabel.1 Delay, Power consumption and area calculation

Topology	SUB Blocks	Delay (ns)	Slices Used (Area)	Power dissipa-tion (10^{-9} W)	PD
Cnt.unit	Decoder	6.275	8	0.081	0.508
ALU	AND	5.753	4	0.081	0.463
	NAND	5.753	4	0.081	0.463
	NOR	5.753	4	0.081	0.463
	XOR	5.753	4	0.081	0.463
	CLA	7.732	5	0.081	0.626
	Inverter	6.034	4	0.081	0.488
	AND	6.546	4	0.081	0.530
	OR	7.508	14	0.081	0.608
USR	MUX	6.582	9	0.081	0.533
BSR	MUX	7.198	16	0.081	0.583
GPR	D-FF	6.546	4	0.081	0.530
TOTAL		77.43	80		6.258

The pipeline stages for different type of instructions that the data memory stage of the pipeline is not used by any of the arithmetic instructions. Transition during this unused state causes extra power dissipation. The pipeline is reconfigured to bypass this stage for these set of instructions. Hence data obtained from execution stage is forwarded directly to the write back stage. During this time, the EXE/MEM pipeline registers are maintained at zero value thus ensuring that no transition take place and power dissipation is reduced.

IV. AREA AND POWER MEASURE REQUIREMENT:

The performance of MIPS processor based on three different modules such as TDES, DES, and AES algorithms. For TDES and DES, 16 clock cycles are used for DES/TDES specific block to execute data, 20 clock cycles are needed to execute the R-type instruction, 21 clock cycle are needed for I-type instruction and 19 clock cycle for J-type instruction data. The consumption of power can be further reduced by running the processor at lower voltages than the normal voltage of 1.5v .This is performed for both the encryption and decryption process. Clock gating technique is used to minimize energy reduction during pipeline stall stages. This technique identifies low processing requirement periods and reduces operating voltage with clock frequency (voltage-frequency scaling), resulting in reduced average power consumption. It may or may not occur frequently depending upon compiler efficiency. Execution per second .The formula for calculating throughput is: Throughput = f * symbol width/total clock frequency .show the performance throughput, area and the estimated power consumption of TDES and DES MIPS processor.

V. RESULT SIMULATIONS:

The ISA of the 64- bit RISC processor was described using the VHDL Code .The tool chain including the Active HDL simulator; it was synthesized using Xilinx ISE. The total memory utilization is 81,408 kB. Maximum combinational path delay is 2.677ns and utilized Operating clock frequency is 300 MHZ.

Fig.2 (a)

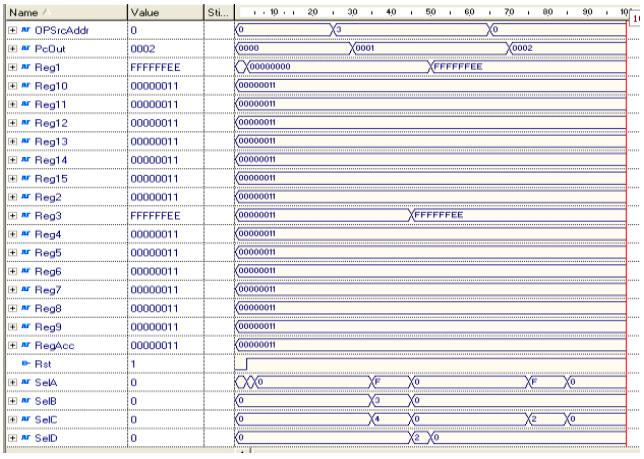

Fig.2. (a) and (b) Simulation Result of 64-bit RISC Processor

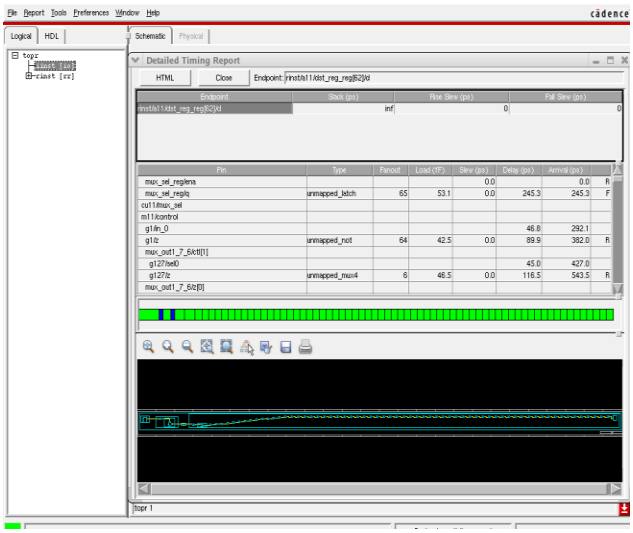

Fig.3. Timing Report

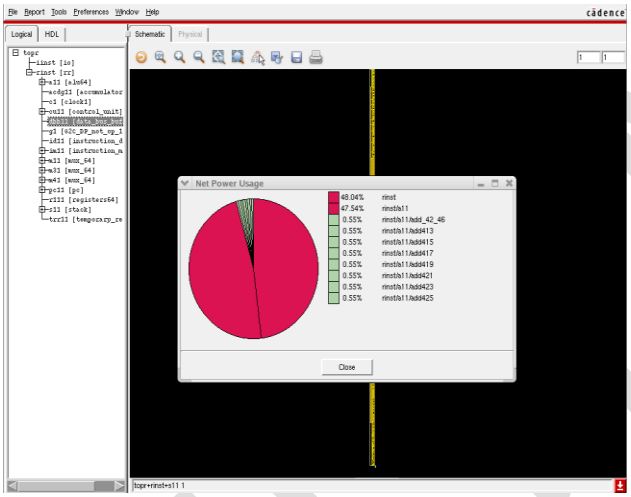

Fig.4. Utilized Net power

VI. Conclusions:

We have implemented 64-bit RISC Processor on Xilinx ISE and the analysis has been done on IUS for FPGA. The design has been achieved using VHDL and simulated with IUS. Future work will be added by increasing the number of instructions and make a pipelined design with less clock cycles per instruction and more improvement in design.

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