Network on a Chip

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Abstract: - A number of research studies have demonstrated the feasibility and advantages of Network-on-Chip (NoC) over traditional bus-based architectures. This whitepaper summarizes the limitations of traditional bus-based approaches, introduces the advantages of the generic concept of NoC, and provides specific data about Arteris' NoC.

Keywords: - Network-on-Chip, System on Chip.

1. INTRODUCTION

By adding many computing resources such as CPU, DSP, specific IPs, etc to build a system in System-on-Chip, its interconnection between each other becomes another challenging issue. In most System-on-Chip applications, a shared bus interconnection which needs an arbitration logic to serialize several bus access requests, is adopted to communicate with each integrated processing unit because of its low-cost and simple control characteristics. However, such shared bus interconnection has some limitation in its scalability because only one master at a time can utilize the bus which means all the bus accesses should be serialized by the arbitrator. Therefore, in such an environment where the number of bus requesters is large and their required bandwidth for interconnection is more than the current bus, some other interconnection methods should be considered.

Such scalable bandwidth requirement can be satisfied by using on-chip packet-switched micro-network of interconnects, generally known as Network-on-Chip (NoC) architecture. The basic idea came from traditional large-scale multi-processors and distributed computing networks. The scalable and modular nature of NoCs and their support for efficient on-chip communication lead to NoC-based system implementations. Even though the current network technologies are well developed and their supporting features are excellent, their complicated configurations and implementation complexity make it hard to be adopted as an on-chip interconnection methodology. In order to meet typical SoCs or multi-core processing environment, basic module of network interconnection like switching logic, routing algorithm and its packet definition should be light-weighted to result in easily implemental solutions.

Whether you are using AXI, OCP, AHB or a proprietary protocol, Flex NoC Network on Chip (NoC) IP reduces the number of wires by nearly one half, resulting in fewer gates and a more compact chip floor plan. Having the option to configure each connection's width, and each transaction's dynamic priority, assures meeting latency and bandwidth requirements.IP configuration tool suite, design and verification can be done easily, in a matter of days or even hours.

2. BENEFITS OF ADOPTING NOCS

NoC links can reduce the complexity of designing wires for predictable speed, power, noise, reliability, etc., thanks to their regular, well controlled structure. From a system design viewpoint, with the advent of multi-core processor systems, a network is a natural architectural choice. A NoC can provide separation between computation and communication, support modularity and IP reuse via standard interfaces, handle synchronization issues, serve as a platform for system test, and, hence, increase engineering productivity

3. BENEFITS OF ADOPTING NOC

- Point-to-Point connections.
- Physical design viewpoint.
- NoC links can reduce the complexity of designing wires for predictable speed, power, noise, reliability, etc.

4. NOC ARCHITECTURE

- Synchronous bus limitations lead to system segmentation and tiered or layered bus architectures.
- Modern Systems-on-Chip (SoCs) today contains hundreds of Intellectual Properties (IPs)/cores, including, programmable processors, co-processors, accelerators, application-specific IPs, peripherals, memories, reconfigurable logic, and even analog blocks. We are now entered in the so called many-core era.
- NoC provides enhanced performance (such as throughput) and scalability in comparison with previous communication

Architecture

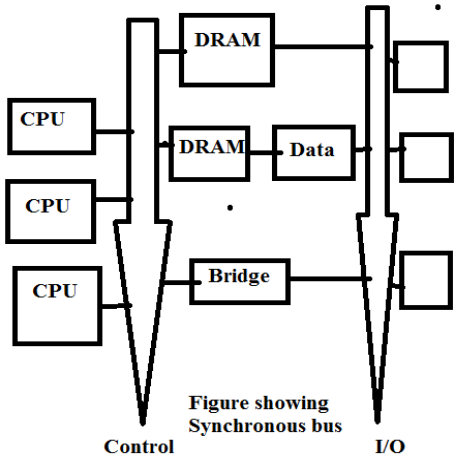

Figure showing Synchronous bus

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