Design Techniques for Low power Op-Amp

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Abstract **- Now a day in electronic design field, the trend is moving towards the low power chip systems. Thus, the demand of smaller size of equipments, chips, with very less power dissipation is needed. In portable equipments, smaller size and longer life of battery is required. Generally, for the reduction of power consumption of any system, the supply voltage must be reduced. Also, some low power design techniques must be employed. Here, in this paper, the various low power techniques for design of Operational Amplifier (Op-Amp) are discussed.**

Index Terms - Operational Amplifier (Op-Amp), Low-Power, Low- Voltage, Weak Inversion.

I. INTRODUCTION

Operational Amplifier (Op-Amp) is the basic building block of any analog electronic circuit or system. Now a day, Op-Amps are vastly utilized in digital circuits also. As per the requirement of present scenario Op-Amps must have very low power consumption with a very high driving capability. The amplifier section of Op-Amp must dissipate less power. Low power amplifier is used to reduce the dissipation of heat and energy is saved in the battery operated equipments. Low power designing techniques for analog circuitry can be done by using one of the following methods and techniques which are discussed one by one later.

1. Bulk-Driven Method
2. FCG MOS Technique
3. Current Driven Bulk (CBD) Technique
4. Weak Inversion MOS Transistor Technique .

II. BULK DRIVEN METHOD

As we know that the reverse bias at source junction increases the threshold voltage and forward bias decreases the threshold voltage. In the previous analog circuits, the transistors are available with three terminals with one extra terminal is either connected to ground (GND) or VDD or tied to the source terminal. Now, it has been found that this bulk terminal is used as a small signal input which is proved to be very suitable for the ultra-low supply requirement.

In the bulk driven MOSFET, firstly we have to bias the gate terminal to create conduction channel inversion layer. To create the inversion layer sufficient voltage is to be given i.e. VGS> VT i.e. voltage between gate-to-source terminal must be greater than the threshold voltage (in case of NMOS). The operation involved in the bulk driven MOSFET is of depletion type.

The main advantage of a bulk driven MOSFET is that the threshold voltage limitations are eliminated and both positive and negative bias voltages are possible over the gate driven MOSFET.

There are also some drawbacks of bulk-driven devices compared to gate-driven devices, such as smaller trans-conductance (gab instead of gm) because of smaller control capacitance of the depletion layer, larger parasitic capacitance to the substrate, which results in lower transfer function and higher input referred noise, because of smaller trans-conductance.

Thus we can say that, the bulk driven amplifier input stage allows a rail-to-rail input common mode voltage range, with substantial gain, at the cost of some extra power dissipation and a large bulk bias dependent input capacitor.

Also, it's to be noted that there's only one type of bulk-driven devices available (PMOS in n-well or NMOS in p-well) depending on the process used.

Unfortunately, the favorable properties of the Bulk driven input stage don't come while not their drawbacks. The input common mode voltage VBS is increasing, whether for the purposes of increasing the gain of the Op Amp, or just to achieve rail-to-rail input common mode, comes at the price of power dissipation

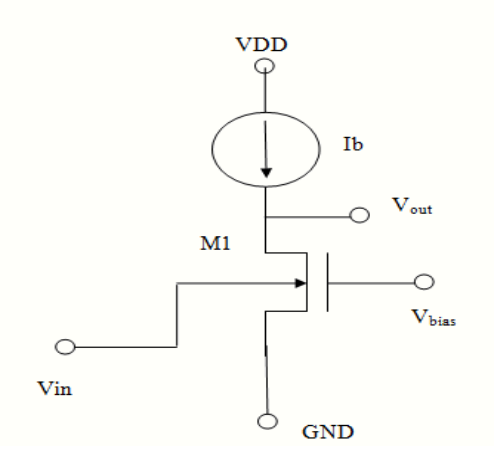

Figure1. Bulk-Driven MOS Transistor

III. FLOATING GATE TECHNIQUE

Floating gate transistors are mainly used in EPROM & EEPROM circuits. FCGMOS transistor is AC coupled at the

gate terminal. It has charge placed on the gate using either UV radiations or high voltage pulses (e.g. 20V), which helps in biasing of the device up to the desired level. In floating gate transistor, the charge on the gate of MOSFET is controlled by two or more inputs through poly-poly capacitor between each input and the floating gate as shown below in the figure

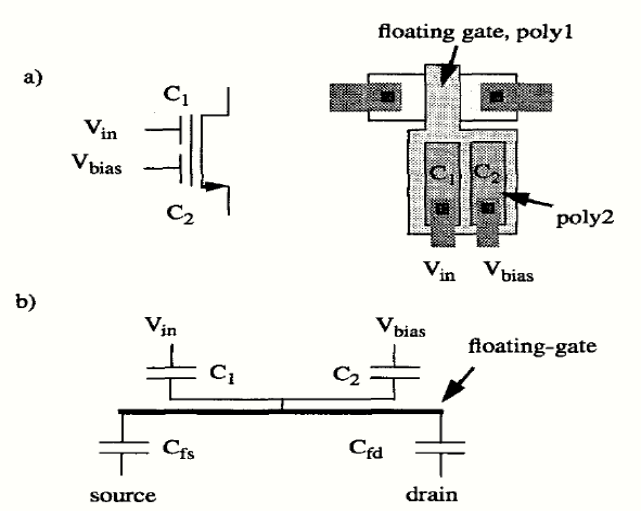

Figure3. Floating Gate MOSFET: (a) Ideal Device (b) Practical Device

During processing a random amount of charge accumulates on the floating-gate causing a change in its potential and in the case of a differential pair an offset since the amount of charge on the two floating-gates may be different. This charge can be removed by grounding the inputs and exposing the poly-poly capacitor edges to shortwave UV-light.
The problem faced by all FGCMOS input devices is that their input coupling capacitors tend to require massive die areas. Therefore, FGCMOS could prove to be an expensive solution to the low voltage supply challenge. Furthermore, placing capacitors at the input of an Op Amp makes it unsuitable for very low frequency operation.
Thus we can say that, the FCGMOS input stage allows a rail-to rail input common mode voltage range, at the cost of limited low frequency capabilities, and large, die area consuming capacitors

IV. CURRENT DRIVEN BULK TECHNIQUE

Current driven bulk technique can be used to achieve low-power & low-voltage design by the reduction in threshold voltage. CBD (Current Driven Bulk) technique is used as means for compensating body effect.
The relationship between threshold-voltage and VBS which is called bulk bias voltage is:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{\left|2\phi_F - V_{BS}\right|} - \sqrt{2\phi_F}\right)$$

Where Vth0 : Zero bias threshold voltage
γ : Bulk effect factor
φF : Fermi potential

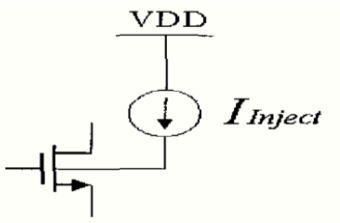

Figure4. NMOS CBD Transistor

Injecting a current into the bulk in NMOS would change the acceptor concentration (NA), which in turn, causes a decrease in the threshold voltage of NMOS. Same understanding is valid for PMOS and donor concentration by extracting an electron from bulk.

V. WEAK INVERSION TECHNIQUE

A simple model for weak inversion is given as:
Where, n is the sub-threshold slope factor and its value of n is greater than 1 and less than 3 and IDo is process dependent parameter.

$$i_D = \frac{W}{L} I_{Do} \exp\left(\frac{v_{GS}}{n(KT/q)}\right)$$

It also depends on and the point at which transistor enters the weak inversion region can be approximated as:
Operation of the-MOS device in sub-threshold region is very important when low power circuits are desired.
From above equation, the trans-conductance can be derived as:

$$g_m = \frac{I_D}{nKT/q}$$

There is linear relationship between trans-conductance and current. Also trans-conductance is independent of device geometry. But in strong inversion relationship between trans-conductance and current is square law and also function of device geometry.

VI. CONCLUSION

All the four techniques discussed above have their own performance & different parameters, and used for different applications. As supply voltages continue to scale down, and performance demands increases, different parameters & low power consideration become important.

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