Designing of DDR SDRAM Controller with User Interface

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***Abstract*— DRAMs have historically been high volume, standard, commodity memories. Today with many high volume applications having differing requirements, DRAMs are becoming more application specific. Today's high-performance CPUs demand high speed memory. Conventional DRAM technology cannot support the data rates that today's CPUs require. As the bus speed gets faster than 50 MHz, new memory devices are required. Synchronous DRAM (SDRAM) is the new memory for high-speed CPUs. DDR SDRAM is similar in function to the regular SDRAM but doubles the bandwidth of the memory by transferring data on both edges of the clock cycles SDRAM is the most prefer able memory for storing large amount of data storage. SDRAM stands for synchronous DRAM in this case all the I/O and control signal of memory is synchronize to clock. In this paper we will understand the DDR-I memory and will also learn the designing steps of the DDR-I controller (kind of SDRAM controller). DDR SDARM controller provides asynchronous command inter face to the DDR SDRAM memory along with several control signals.**

Index Terms:-Memory, SDRAM, DRAM, SDR, DDR-I-II-III, FPGA, VHDL, read, write

I. INTRODUCTION

There is a continual demand for computer memories to be larger, faster, lower powered and physically smaller. These needs are the driving force in the advancement of DRAM (Dynamic random-access memory) technology. Mainstream DRAMs have evolved over the years through several technology enhancements, such as SDRAM (Synchronous DRAM), DDR (Double Data Rate) SDRAM, DDR2 (Double Data Rate 2) SDRAM, and DDR3 (Double Data Rate 3) SDRAM. The bottleneck existed between CPU and memory slows down the improvement in computer performance. Great pressure is put on predictability; also the performance and architectural efficiency of memory are required to be increased.[4]

Double Data Rate (DDR) SDRAMs have been prevalent in the PC memory market in recent years and are widely used for networking systems. These memory devices are rapidly developing, with high density, high memory bandwidth and low device cost. However, because of the high-speed interface technology and complex instruction-based memory access control, a specific purpose memory controller is necessary for optimizing the memory access trade off.[3]

The SDR (*Single Data Rate*) transfers data on only one clock transition (0-1 or 1-0); in contrast to DDR (Double Data Rate), two samples are taken every sample clock. DDR achieves higher bandwidth as by transferring data on both the rising and falling edge of the clock signal is used to allow higher speeds of transfer with slower hardware designs. Like DDR before it, DDR cells transfer data both on the rising and falling edge of the clock (a technique called *double pumping*). The key difference between DDR and DDR2 is that in DDR2 the bus is clocked at twice the speed of the memory cells, so four words of data can be transferred per memory cell cycle. Thus, without speeding up the memory cells themselves, DDR2 can effectively operate at twice the bus speed of DDR. Figure 1 shows the SDR and DDR data transfer with respect to the clock.[8]

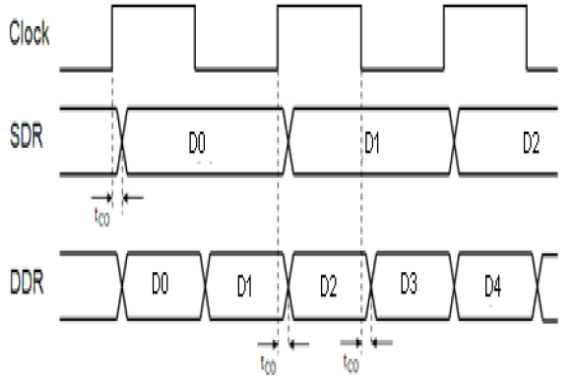

Figure 1. SDR and DDR Timing diagram

Figure 2 shows the logic circuit diagram of SDR and DDR data flow with respect to clock edges. Here for SDR data transfer we used only single flip flop, in this type of mode the data is transfer only falling edges of the clock. In case of DDR data transfer we used two flip flops which outputs are transferred through the 2-to-1 multiplexer.[8]

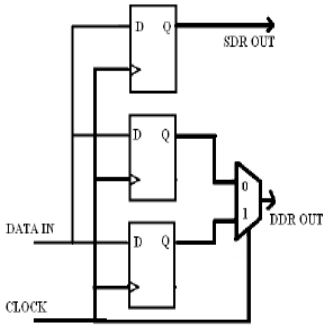

Figure 2. Logic circuit diagram of SDR and DDR data flow with respect to clock edges

II. DDR SDRAM MEMORY AND CONTROLLER

Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) is being implemented broadly in computing platforms and embedded applications.Specifications are defined by the Joint Electronic Devices Engineering Council (JEDEC), but it's up to designers to guarantee compliance. The specification for DDR-I memory is mentioned in the Table-1.

DDR standard	DDR1
Specification	JESD79E
Operating voltage	1.5 - 3.3V
Clock frequency	100 - 200 MHz
Data transfer rate	200 - 400 MT/s
Package type	This Small Outline Package (TSOP)
Package size	x4, x8, x16, x32
Bacward compatibility	No

Table 1. DDR technologies and key JEDEC specifications

The DDR interface consists of signals for control, address, clock, strobe and data. As Figure 3 shows, clock, address and control signals are transmitted one way from the memory controller to the DDR chip; strobe and data signals are bi-directional. In a read operation, the strobe and data signals are transmitted from the DDR chip to the memory controller. In a write operation, the signals move in the opposite direction.

To improve signal performance as data transfer rates increase and signal amplitude decreases, the clock and strobe signals are differential, which cancels out common mode noise. The other signals still operate in single-ended mode, which makes them more susceptible to noise, crosstalk and interference.[7]

DDR SDRAM controller controls the access to memory in accordance with the timing rules, including the control of the read/write control signals, address signals, data signals , power on initialization signals, etc. We can simply the state machine of the controller as shown in Figure 4.Prior to normal operation, DDR SDRAMs must be powered up and initialized in a predefined manner. When initial sequence completed, the design is calibrated to ensure that correct data is captured in the ISERDES primitives. When initialization and calibration is done, the controller set the phy_init_done signal HIGH and the memory is DLE, which is signaled to start normal operation of the design. Now, the controller can start issuing user write and read commands to the memory.

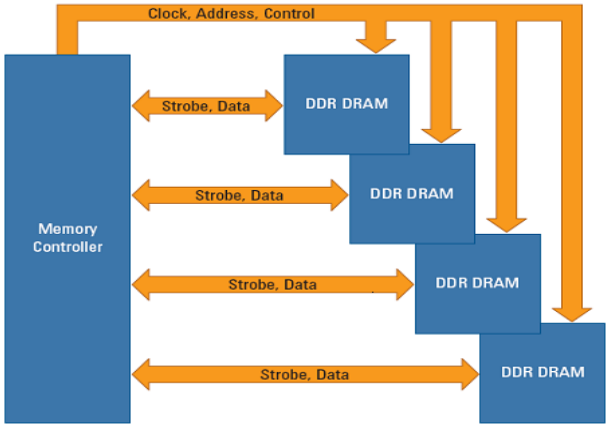

Figure 3. In the DDR Interface, clock, address and control signals move from the memory controller to the DDR chip, but strobe and data signals are bi-directional. Their direction depends on the operation being performed.

In the design of controller, timing control of reading and writing operations is completed according to the state machine. Before issuing a READ or WRITE command, we should active the row to be read or written, as shown in Figure 4. Read and write accesses to the DDR SDRAM are burst-oriented. The burst length determines the maximum number of column locations accessed for a given READ or WRITE command , and the value can be reprogrammable to either 2, 4, or 8. In this design, the burst length is set to be 8 to guarantee the efficiency of read and write.

An AUTO REFRESH command is issued to the DDR memory at specified intervals of time to refresh the charge to retain the data. If the memory is reading or writing when issuing an AUTO REFRESH Command,the controller will wait until the current operation complete and then send a new command. If the user has read/write request during the refresh process, the controller will not respond to the requests until the completion of the current refresh cycle.

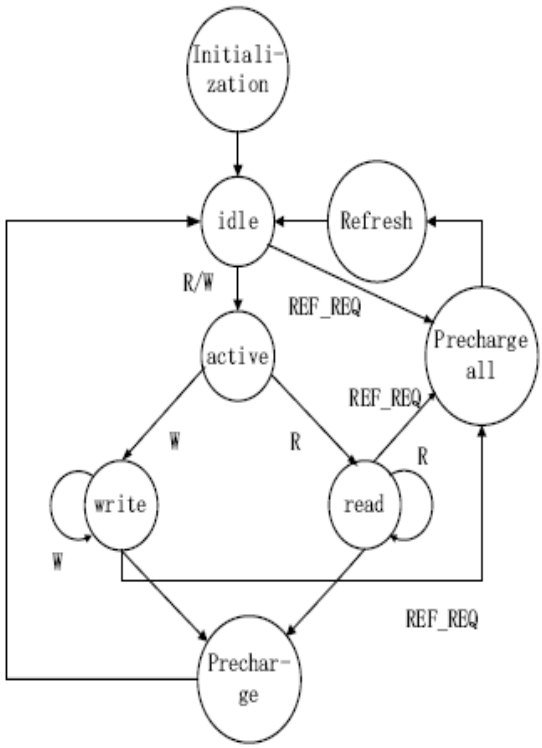

Figure 4. Simplified state machine of DDR SDRAM controller

III. DDR CONTROLLER DESIGNING

DDR design can be segmented into four areas: interconnect design, active signal validation, protocol validation, and functional test. With no formal verification labs or test centers, you must decide the appropriate procedures, methods and equipment to perform these compliance tests.

The controller of the DDR is available but the main part is to design the user interface of the DDR memory according to the user requirement. Xilinx provides the best platform for designing the controller with various FPGA (e.g. Virtex-IV,V) boards.

While designing DDR the voltage level compatibility need to be cared. Double Data Rate (DDR) SDRAM was defined by JEDEC 1997, and it was designed to be a natural migration from PC100 and PC133 SDRAMs to higher data rates(PC266). the VDD and VDDQ supply voltages have been reduced from 3.3V to 2.5V, so the power dissipation of PC266 devices will actually be lower than the power dissipation of PC100 and PC133 devices.

The PC266 motherboard design is very similar to current SDRAM motherboard designs, with the exception of the SSTL_2 signaling. The use of high-speed, low voltage signaling, such as SSTL_2, requires proper termination voltage and reference voltage design. Some attention must be paid to the generation and location of the termination voltage (VTT) and reference voltage (VREF) circuits, and to the placement and routing to the series and parallel termination resistors.[11]

SSTL_2 stands for Series Stub Terminated Logic for 2.5V, and it was also defined and standardized within JEDEC. Although it is applicable for many different applications, SSTL_2 is particularly optimized for the main memory environment, which has long stubs off of the motherboard bus due to the DIMM routing traces.

Table 2details the key parameters of the SSTL_2 specification. Note that the difference between VIH and VIL is now only 0.36V (2 x 0.18V), as compared to 1.2V with LVTTL. Also note that the minimum output voltage swing can be as small as 0.70V. VREF is defined as 50% of VDDQ, as VDDQ can vary from 2.3V to 2.7V. In PC266 configurations, VREF will be generated with 1% accuracy. The termination voltage, VTT, is defined as being within 40mV of VREF. The goal for the VREF and VTT circuits is to generate the VREF and VTT voltages that can track the midpoint of VDDQ – VSSQ over environmental variations, and to be symmetric with respect to VOH and VOL. The VREF and VTT voltages must also track each other.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DD}	Device Supply Voltage	V_{DDQ}		n/a	V
V_{DDQ}	Output Supply Voltage	2.3	2.5	2.7	V
V_{REF}	Input Reference Voltage	1.15	1.25	1.35	V
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V
INPUT DC LOGIC LEVELS					
V_{IH} (DC)	DC Input Logic High	V_{REF}+0.18		V_{DDQ}+0.3	V
V_{IL} (DC)	DC Input Logic Low	-0.3		V_{REF}-0.18	V
INPUT AC LOGIC LEVELS					
V_{IH} (AC)	AC Input Logic High	V_{REF}+0.35			V
V_{IL} (AC)	AC Input Logic Low			V_{REF}-0.35	V
OUTPUT DC CURRENT DRIVE					
I_{OH} (DC)	Output Minimum Source DC Current	-15.2			mA
I_{OL} (DC)	Output Minimum Sink DC Current	15.2			mA

Notes: V_{REF} and V_{TT} must track variations in V_{DDQ}.
Peak-to-peak AC noise on V_{REF} may not exceed ±2% V_{REF} (DC).
V_{TT} of transmitting device must track V_{REF} of receiving device.

Table 2. SSTL_2 Key Specifications [12]

Traditionally, logic systems have been designed to clock data on only one edge of the clock, while the new double data rate (DDR) memories clock on both the leading and falling edges of the clock. This doubles the data rate while slightly increasing system power dissipation.

The increased data rate requires that the clock distribution network be carefully designed to minimize ringing and reflections that can inadvertently clock logic devices. Two possible bus termination schemes are presented in Figure 5. In Figure 5a, bus termination resistors are placed at the end of the distribution network and are connected to ground. If the bus driver is in the low state, the resistors have zero dissipation. In the high state, the resistors dissipate power equal to the supply voltage (VDD) squared divided by the bus resistance. With a random voltage on the bus, the average loss is the supply voltage squared divided by twice the bus resistance.

In Figure 5b, the termination resistor is connected to a supply voltage (VTT) that is one-half the VDD voltage. The dissipation in the termination resistor is then constant regardless of the supply voltage and is equal to VTT [or (VDD/2)] squared divided by the termination resistance. This results in a factor of two power savings when compared with the first approach (in case a bus signal is high 50% of the time and low 50% of the time), but at the cost of an additional power supply. The requirements of this power supply are a little unique. First, its output needs to be one-half the driver voltage (VDD). Second, it needs to both source and sink current. When the driver output voltage is low, current flows from the VTT supply into the driver. However, when the driver is high, current flows from the driver into the supply. Third, the supply needs to go from either operating mode into the other mode as the system data changes.

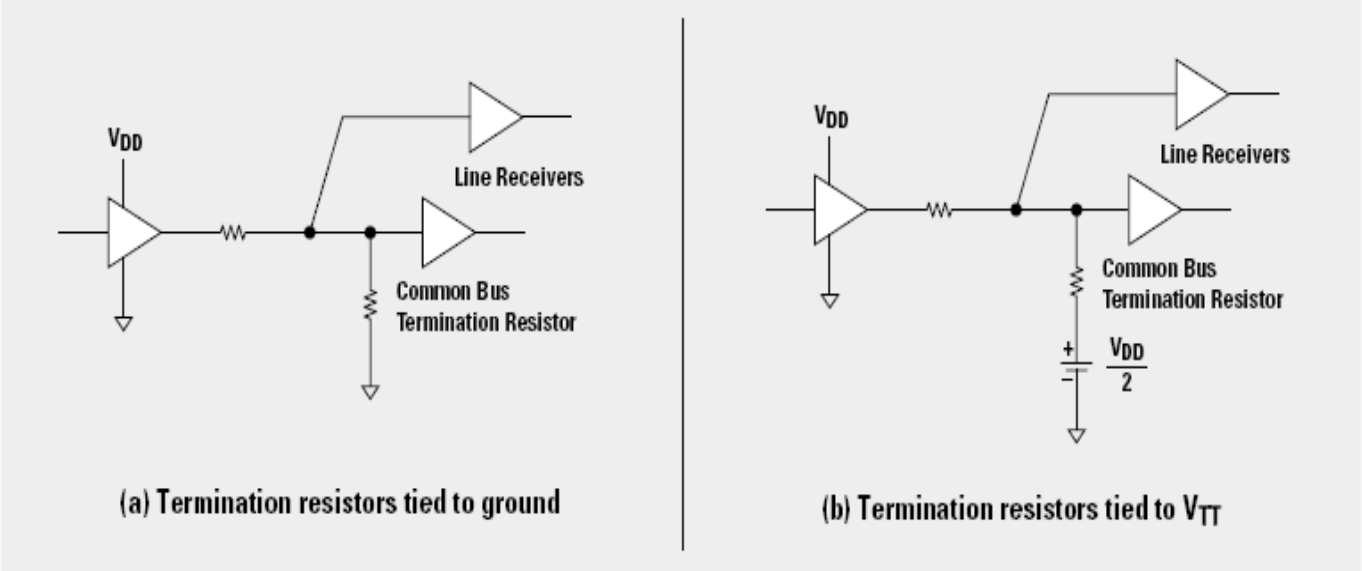

Figure 5(a). Bus Termination Scheme [12]

Figure 5(b). Bus Termination Scheme [12]

The termination regulator voltage is essential part of designing DDR controller. The regulator IC is provided by many manufacturer like Texas Instrument, Linear Technology etc. Among them the designer can use any relevant IC for the designing.

IV. SIMULATION RESULT

DDR controller simulation result is shown below.

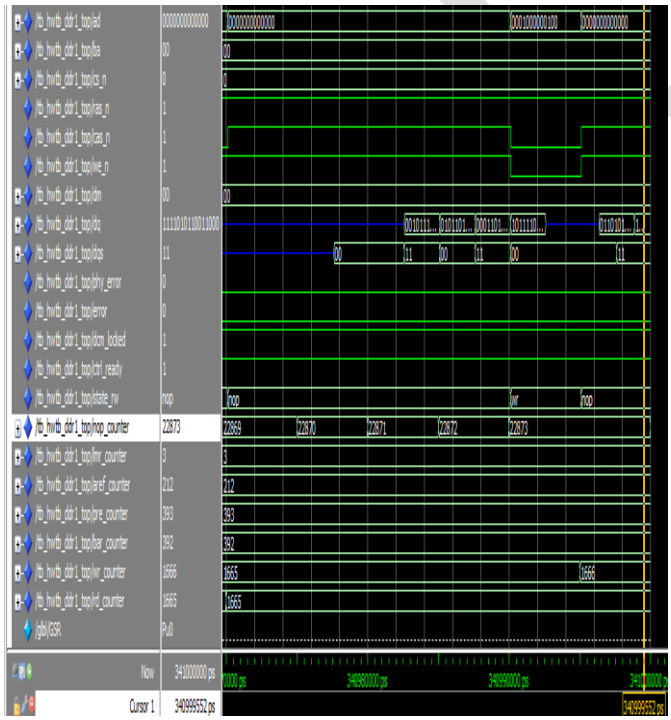

Figure 6 Case-I

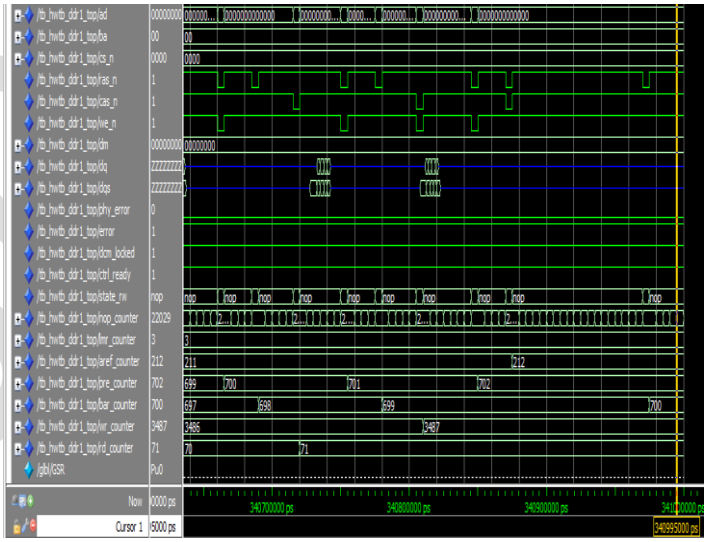

Figure 7 Case-II

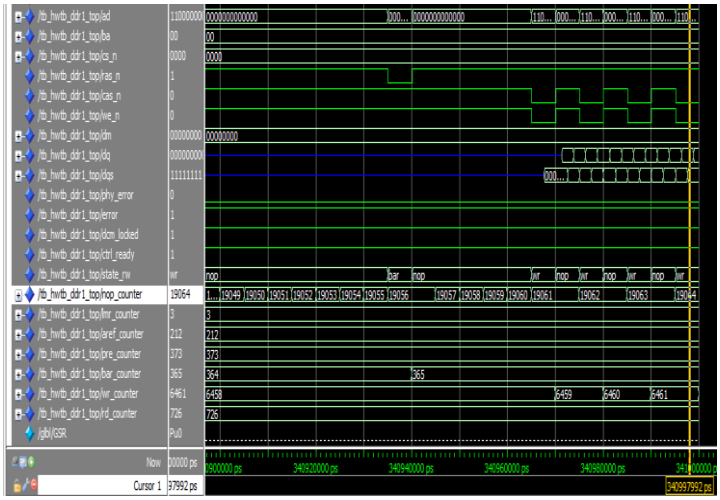

Figure 8 Case-III

Parameters	Result till now(Case-I)	Result achieved with better performance(Case-II)	Result achieved (Case-III)
Write counter	1665	3487	6461
Read counter	1665	71	726
NOP counter	22873	22029	19064
Ratio of NOP to Write-Read counter	6.86	6.1	2.65
Design Specification	Burst length-4 Data width-16 No of comps-1	Burst length-4 Data width-64 No of comps-4	Burst length-4 Data width-64 No of comps-4

Table 1 Comparison of the different simulation result.

CONCLUSION

This paper gives deep knowledge about the DDR SDRAM controller designing. The designing parameters like termination voltage, user interface need to be taken care while designing the DDR controller. To design the DDR controller not only the knowledge of DDR controller is required but also the knowledge of the signaling, termination and reference voltages of DDR are required.

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