Cascade Multilevel Inverter A System Friendly Supply and Its MATLAB Modeling

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***Abstract*: One of the biggest problems in power quality aspects is the harmonic contents in the electrical system. Many industrial applications which may allow a Harmonic content of 5% of an input voltage inverter output voltage of harmonic content 5% high. In Multilevel Inverter it is possible to obtain refined output voltage wave forms and reduced THD in voltage with increased number of voltage levels i.e. by using stepped output voltage waveform. This paper discuss about the problems in conventional two level inverter and how these problem can be overcome by multilevel inverter. This paper describes the simulation model and harmonics analysis of cascade H-bridge Inverter fed RL load. The simulation and harmonic analysis of the proposed inverter will be discussed and the total harmonic distortion will be evaluated. The simulation studies on the proposed scheme have been obtained through the MATLAB/SIMULINK software.**

Key Words: Cascaded H-bridge multilevel inverter, MATLAB Simulink, THD.

I.INTRODUCTION

The demand for control of electrical power for electrical motor drives is increasing day-by-day with the industrial growth around the globe. Induction Motor (IM) is the workhorse of the industry because of the simplicity of construction and ruggedness offered by it. Inverter fed IM based Adjustable Speed Drives (ASD) needs efficient control of both voltage and frequency. The PWM inverter reduces the amplitudes of lower order harmonics in the motor terminal voltage by shifting the dominating harmonics towards higher frequencies. The power devices in conventional are switched at high frequency to realize the output voltage at the reference fundamental frequency as demanded by the PWM controller. These inverters produce pulsed output voltage waveforms, at the motor terminals, which contain a fundamental component and other harmonic components centred on the switching frequency and its multiples. Hence, a higher switching frequency is desirable, as it is relatively easier to filter out the harmonic component at higher frequency compared to the component at the lower frequency. Higher switching frequencies lead to better output voltage and current waveforms, reduced harmonic currents and faster control of the drive.

Even though, switching the PWM-VSI fed ASD at higher frequencies results in improvement in the overall performance of the drive, it causes significant amount of switching losses and generates conducted as well as radiated electromagnetic interference (EMI). As the two-level inverters have to switch between the two extreme levels of the dc-link voltages, they involve large voltage change rates (dv/dt) in every switching. This dv/dt effect can result in additional EMI and increased stress on the insulation of the machine windings. This large dv/dt also appears in the alternating common-mode voltage (CMV) generated by the PWM controlled two-level inverters and can cause the motor shaft voltages, flow of motor bearing currents and consequently increased ground leakage currents. Also, in a two-level inverter, each device has to be rated to block the entire dc-link voltage during its off time. So, when used for high-voltage and high-power drive applications, the conventional two-level inverters experience above mentioned limitations. Therefore, in practice, use of conventional two-level inverters employing PWM techniques is restricted to low and medium power applications.

For the high-voltage high-power industrial drives, PWM-VSIs operating at high switching frequencies are seldom preferred due to considerable switching losses. Thus, the task of reducing harmonic contents in the output voltage has to be addressed in a different way for PWM-VSI fed IM drives, especially for high-voltage high-power applications. This has been made possible by the use of different class of PWM inverters, termed as multi-level inverters. Multi-level inverters are realized from a number of smaller discrete voltage sources, and they generate the output voltage waveforms with more steps of smaller magnitudes. Significant inherent advantages offered by the multi-level inverters compared to their two-level counterparts. Although multilevel inverters are designed initially to reduce the harmonic contents in the output voltage waveforms, the multi-level inverters have very quickly established themselves as a preferred option for realizing high-voltage high-power drives for industrial, marine, utility and traction applications, using power devices of lower voltage ratings. Today, multi-level inverters are extensively used in high-power drive

applications for laminators, mills, conveyors, pumps, fans, blowers, compressors, etc.

II. MULTI LEVEL INVERTER

The term multilevel began with the three-level converter. Multilevel inverter generates output voltage with stepped waveforms by using an array of power semiconductors and capacitors voltage sources. The commutation of switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig. 1 shows the schematic of one phase leg of inverters with different number of levels, for which the action of power semiconductors is represented by an ideal switch with several positions.

For a three-level inverter, as shown in Fig 1(a), the pole voltage level –Vdc/2, 0, andVdc/2can be attained with corresponding switching function values 0,1, and 2, respectively. In a similar way, for a five-level inverter, the pole voltage level-Vdc/2,-Vdc/4,0,Vdc/4 and Vdc/2 can be attained with switching function value 0,1,2,3, and 4, respectively as shown in Fig. 1(b). For a general n-level inverter, the switching function has a range from 0 to n-1, a shown in Fig. 1(c).

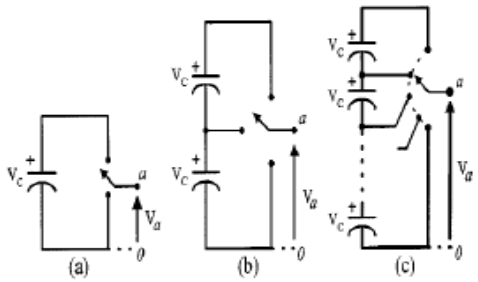

Fig. 1.: Representation of one leg (pole) of an inverter: (a) three level, (b) five level, and (c) general n-level.

A three level inverter generates an output voltage with three values, and a five level inverter generates five voltages, and so on.

Considering that m is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load k is

$$k = 2m + 1 \qquad (1)$$

and the number of steps p in the phase voltage of a three-phase load in wye connection is

$$p = 2k - 1 \qquad (2)$$

The multilevel inverters are classified into three types

1) Diode-clamped [1];
2) Capacitor-clamped [2], [3], [4];
3) Cascaded H-Bridge [2], [5]-[7].

The significant advantages offered by the multi-level inverters compared to conventional two level inverter are listed as follows:

- It is possible to use power semiconductor devices of lower voltage ratings to realize high voltage levels at inverter output;
- It is possible to obtain refined output voltage waveforms and reduced *total harmonic distortion* (THD) in voltage with increased number of voltage levels (stepped output voltage waveforms);
- It is possible to obtain machine currents with reduced harmonics, resulting into reduced torque pulsations in the drive system;
- It is possible to reduce the EMI problems by reducing the switching *dv/dt*;
- Lower amplitudes of alternating CMV and hence lower bearing currents;
- Less stress on the insulation of machine phase windings;
- Inverter can be operated with the lower switching frequency and hence the switching losses are reduced.

III. CASCADED H-BRIDGE INVERTER

Multi-level inverter structures can be realised by cascading (connecting in series) several single phase H-bridge structures with separate dc sources. Fig. 2, shows a cascade multi-level inverter configuration which consists of two cascade cells for each phase and results into a five-level inverter structure. Each cascaded cell consists of the full bridge inverter fed from an isolated rectifier.

The output from each cell is like a three-level single-phase inverter and can attain any of the three values $V_{dc}/2$, 0 or -$V_{dc}/2$, depending upon the states of the switches (two switches in each leg form a complementary pair, e.g., S_{11} and S_{14}, Fig. 2). For example, in a cell, when switch S_{11} and S_{12} are switched ON, the output voltage is equal to -$V_{dc}/2$, when S_{13} and S_{14} are turned ON, the output voltage is equal to $V_{dc}/2$, and when S_{11} and S_{13} or S_{14} and S_{12} are turned ON, the out voltage of the cell is 0. Thus depending on the states of switches in the phase-A inverter cells, the pole voltage of phase-A can be either V_{dc},$V_{dc}/2$, 0,-$V_{dc}/2$, or -V_{dc}, thus forms a five-level inverter structure. In general, the number of steps in the output pole voltage for cascaded inverter structure is given by $n=2m+1$, where m is number of isolated dc supplies per phase.

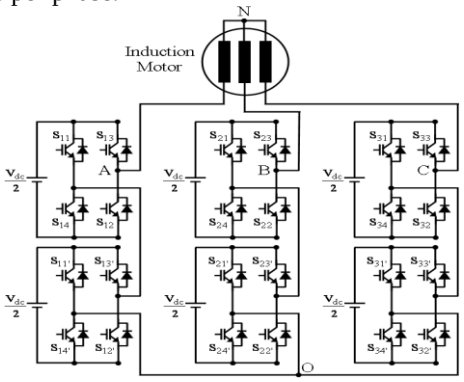

Fig. 2: Cascaded H-bridge five-level inverter configuration

Such (n-1)/2 H-bridge cells, each one having separate dc source of $V_{dc}/(n-1)$, can be sequentially connected to achieve one leg of an n-level inverter

This type of cascaded inverters has become popular in high-power drive applications because of their modular structure and simplicity of control. They are particularly attractive for large electric drive applications where separate dc sources are available in large numbers in the form of batteries. The inverter structure is very simple as each inverter cell has identical structure and thus the extension to higher levels does not add any more power-bus complexity. Also the complicacies like, the capacitor voltage balancing, or clamping diodes/capacitors etc. are not required. The limitation of this topology is the requirement of large number of separate dc sources. But if the dc power supplies are supplied through phase shifted transformers, very good power quality can be achieved at the utility side.

IV. MATLAB SIMULATION AND RESULT DISCUSSION OF CHB-MLI

Figure 3 shows the three phase MATLAB Simulink model of a 7 level CHB. Figure 4 shows the control circuit used for this circuit. And the values of repeating sequence block which is used for carrier wave generation is shown in figure 5. Figure 6 to Figure 10 shows the line voltage wave form of a 7 level, 9 level, 11 level, 13 level and 23 level CHB respectively. It is clear from fig 6-10 that as the number of level increases is output voltage waveform become more sinusoidal.

The value of supply voltage Vdc is 100V, modulation index is 1. The THD values of 7 level to 13 level and 23 level are 9.74%, 7.64%, 6.42%, 5.04% and 4.16% respectively.

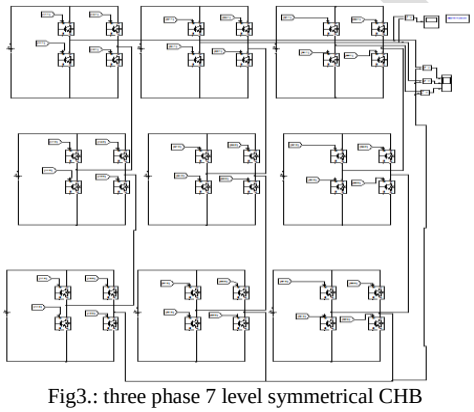

Fig3.: three phase 7 level symmetrical CHB

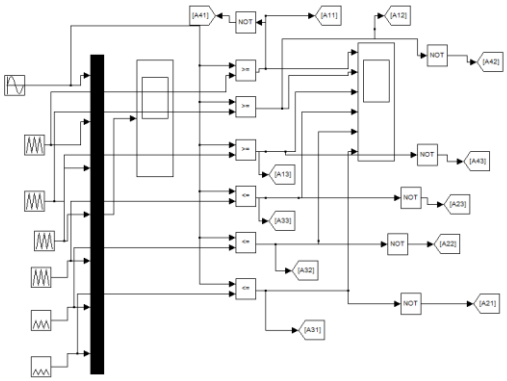

Fig.4.: firing circuit for phase A 7 level symmetrical CHB.

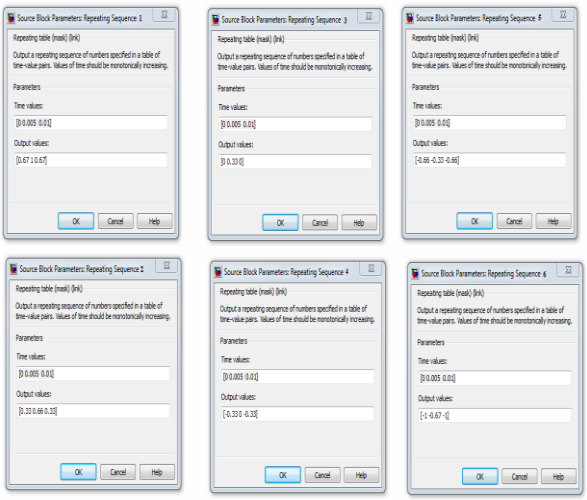

Fig.5 :Values of Repeating sequence block.

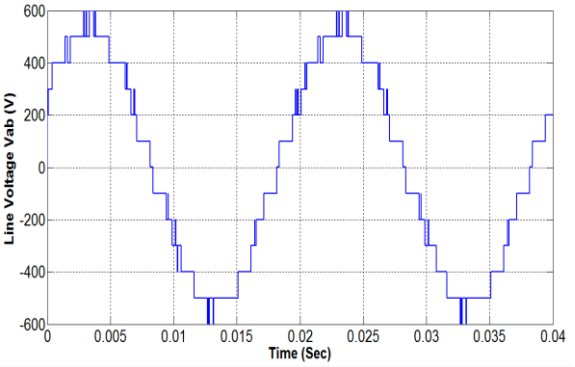

Fig. 6: Line voltage Vab of 7 level CHB.

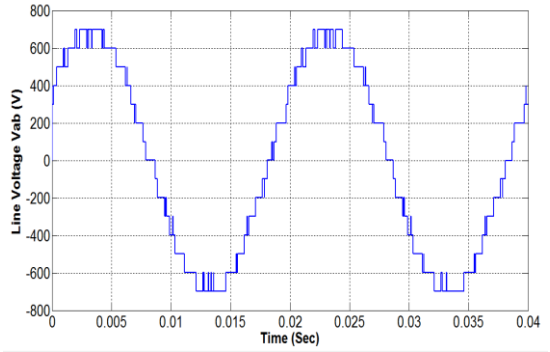

Fig. 7: Line voltage Vab of 9 level CHB.

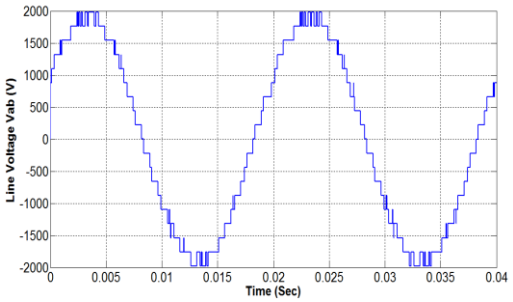

Fig. 8: Line voltage Vab of 11 level CHB

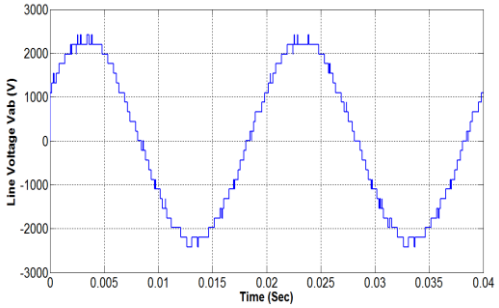

Fig. 9: Line voltage Vab of 13 level CHB.

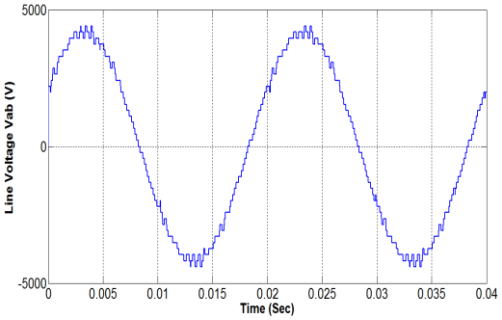

Fig. 10: Line voltage Vab of 23 level CHB.

V. CONCLUSION

Multi-level inverters are the preferred choice in industry for the application in High voltage and High power application. Multilevel inverters fulfil the task of reducing the harmonic contents in the output voltage waveforms. As the number of level increases the THD values in output voltage waveform is decreases. Also the CHB requires the least number of components among all multilevel converters to achieve the same number of voltage levels. The series of H-bridge facilitates modularizes layout and packaging. This enables the manufacturing process to be completed more quickly and cheaply.

REFRENCES

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Applicat. , vol. IA-17, pp. 518–523, Sept./Oct. 1981.

[2] J. S. Lai and F. Z. Peng, "Multilevel converters–A new breed of power converters," IEEE Trans. Ind. Applicat. , vol. 32, pp. 509–517, May/June 1996.

[3] T. A. Meynard and H. Foch, "Multi-level choppers for high voltage ap-plications," Eur. Power Electron. Drives J. , vol. 2, no. 1, p. 41, Mar. 1992.

[4] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison of multilevel inverters for static var compensation," inConf. Rec. IEEE-IAS Annu. Meeting , Oct. 1994, pp. 921–928.

[5] P. Hammond, "A new approach to enhance power quality for medium voltage ac drives," IEEE Trans. Ind. Applicat., vol. 33, pp. 202–208, Jan./Feb. 1997.

[6] E. Cengelci, S. U. Sulistijo, B. O. Woom, P. Enjeti, R. Teodorescu, and F. Blaabjerge, "A new medium voltage PWM inverter topology for adjustable speed drives," in Conf. Rec. IEEE-IAS Annu. Meeting, St. Louis, MO, Oct. 1998, pp. 1416–1423.

[7] R. H. Baker and L. H. Bannister, "Electric power converter," U.S. Patent 3 867 643, Feb. 1975.