Implementation of Image Edge Detection Using FPGA

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***Abstract*-The proposed work presents FPGA based architecture for Sobel edge detection operator. It has found application in forensic science and also in digital multimedia for creating image dazzling effect. Currently the image processing algorithms are limited to software implementation which is slower due to the limited processor speed. So a dedicated processor for edge detection and was required which was not possible until advancement in VLSI technology. Now more complex system can be integrated on a single chip providing a platform to process real time algorithms on hardware. Sobel operator is chosen due to its property of less deterioration in high levels of noise. A lot of research work is in progress in various areas resulting in many computationally efficient algorithms. The choice of the technique in most cases depends on the application and image in question rather than a generalized method. The objective of this Paper is to realize the edge detection algorithm on FPGA. FPGA implementation renders it more useful for real time applications.**

Keywords: FPGA, VLSI, edge detection, Sobel operator

I. INTRODUCTION

Field Programmable Gate Array (FPGA) technology is become an alternative for the implementation of software algorithms. The unique structure of the FPGA has allowed the technology to be used in many applications from video surveillance to medical imaging applications. FPGA is a large-scale integrated circuit that can be re-programmed. The term "field programmable" refers to ability of changing the operation of the device. Gate array refers to the basic internal architecture that makes re-programming possible. Implementations of real-time image processing algorithms can be done on general purpose microprocessors. In certain instances, image processing algorithms are also implemented using digital signal processors and application specific integrated circuits. The application of FPGA in image processing has a large impact on image or video processing. This is due to the potential of the FPGA to have parallel and high computational density as compared to a general purpose microprocessor. This is coupled together with the ability of FPGA of being re-programmable that adds flexibility in the development of image processing algorithms on FPGA. During the recent years FPGAs have become the dominant form of programmable logic. In comparison to previous programmable devices like PAL and CPLDs, FPGAs can implement far larger logic functions. FPGAs support sufficient logic to implement complete systems and sub-systems. FPGA exploit the increasing capacity of integrated circuits to provide designers with reconfigurable logic that can be programmed on application-specific basis. This drastically increases flexibility in both the design process and the final artifact by permitting one board-level design to perform many functions or to be upgraded in the field.

A. Edge Detection:

Edges are one of the most important elements in image analysis and computer vision because they play quite a significant role in many applications of image processing in particular for machine vision. A lot of computer vision methods rely on edge detection as a pre-processing stage. However no single edge detection algorithm can successfully discover edges for diverse images and no specific quantitative measure of the quality for edge detection is given at present. Conventional edge detection mechanisms examine image pixels for abrupt changes by comparing pixels with their neighbours. This is often done by detecting the maximal value of gradient such as Roberts, Prewitt, Sobel, Canny and so on all of which are classical edge detectors. Alternatively we can detect the zero-crossing points. Laplacian and MAR algorithms are based on the idea. Mallat established the edge detection technique in a multi-scale manner using the dyadic wavelet transform. Smallscaled transform filters are sensitive to edge signals but also prone to noise while large scaled filters are robust to noise but could filter out fine details. Recently many multi-scale transform tools based on statistics have been developed.

In early processes the edge detection was mainly performed on software due to its large hardware requirement and also the application-specific integrated circuits have not gain much advancement. But present researches on programmable devices make it possible to implement edge detection algorithms on these devices whose design turn-around time varies from few hours to few days. The goal of edge detection is to mark the points in a digital image at which the luminance changes abruptly. Edge detection is a method of determining the discontinuities in gray level images. Edge detection is essentially a set of connected pixels that lie on the boundary of two regions that are in the gray scale color space.

II. IMPLEMENTATION OF IMAGE EDGE DETECTION USING FPGA

The edges of image are considered to be most important image attributes that provide valuable information for human image perception [1-3]. The edge detection is a terminology in image processing particularly in the areas of feature extraction to refer to algorithms which aim at identifying points in a digital image at which the image brightness changes sharply [4-6]. The data of edge detection is very large so the speed of image processing is a difficult

problem. FPGA can overcome it [7]. Sobel operator is commonly used in edge detection. Sobel operator has been researched for parallelism [8] but Sobel operator locating complex edges are not accurate. It has been researched for the Sobel enhancement operator in order to locate the edge more accurate and less sensitive to noise but the software can not meet the real-time requirements [9].

A. Sobel Edge Detection Enhancement Algorithms:

The Sobel operator is a classic first order edge detection operator computing an approximation of the gradient of the image intensity function. At each point in the image the result of the Sobel operator is the corresponding norm of this gradient vector. The Sobel operator only considers the two orientations which are 0°and 90°convolution kernels as shown in Fig. 2.1.

-1	0	1
-2	0	2
-1	0	1
G_x		

-1	-2	1
0	0	0
1	2	1
G_y		

Fig: 2.1 Convolution Kernels In X And Y Direction.

These kernels can then be combined together to find the absolute magnitude of the gradient at each point.

The gradient magnitude is given by:

$$|G| = \sqrt{G_x^2 + G_y^2}$$

Typically an approximate magnitude is computed using:

$$|G| = |G_x| + |G_y|$$

This is much faster to compute. The Sobel operator has the advantage of simplicity in calculation. But the accuracy is relatively low because it only used two convolution kernels to detect the edge of image.

B. FPGA Hardware Implementation:

This design uses 3×3 convolution kernels processing 256×256 Gray Scale Image from the database in personal computer. The architecture is shown in Fig.4.2.The system is divided into four modules: 3×3 pixel generation module, Sobel enhancement operator module, edges control module and binary segmentation [10,11]. In this system, Clk is the clock signal, Reset is the reset signal and EN is data control signal, Data input is the pixel signal of Gray Scale Image, Result is the result of edge detection operator signal, Generation data and Data are the middle signal. The function and structure of each module are as follows:

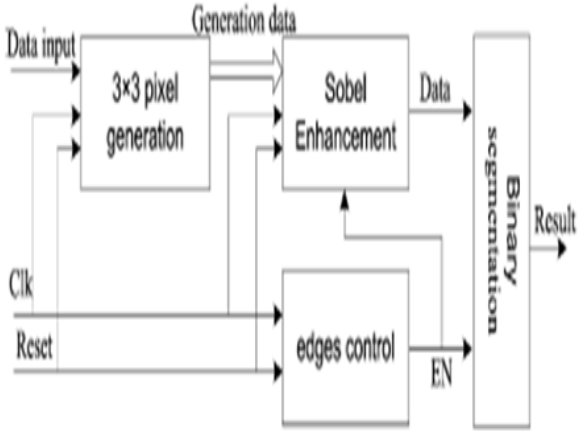


Fig 2.2 Architecture.

1) 3×3 Pixel Generation module: The structure of 3×3 pixel generation module is shown in Fig.4.3. This module consists of 3 shift register groups and two FIFO. The FIFO is used to cache a line of image data. The image data is input according to the clock signal so P1, P2, •••,P9 is the 3×3 image data template. When the data is continuously input 3×3 image data template changes. It can contain all pixels of an image. The FIFO is generated by dual-port RAM [12].

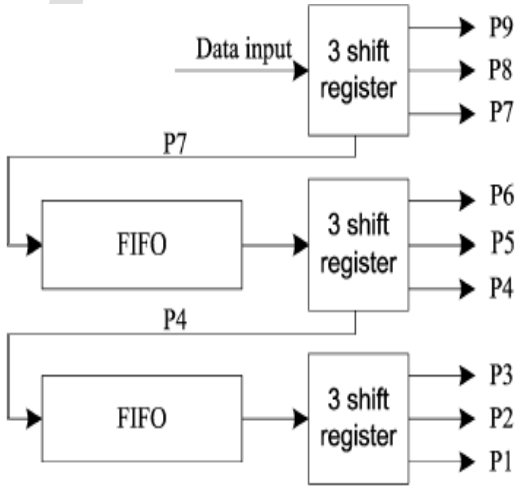


Fig 2.3 3×3 Pixel Generation Module.

2) Sobel Enhancement Operator Module: The structure of Sobel enhancement operator module is shown in Fig 4.4. The parallel processing construction is used in orientation convolution kernel. The orientation convolution result is compared with each other and then the maximum value is the output. The pipeline structure is used to calculate each orientation convolution kernel. It is six corresponding input data because three coefficients of each convolution kernel are zero multiplied by 2. The structure is shown in Fig.4.5.

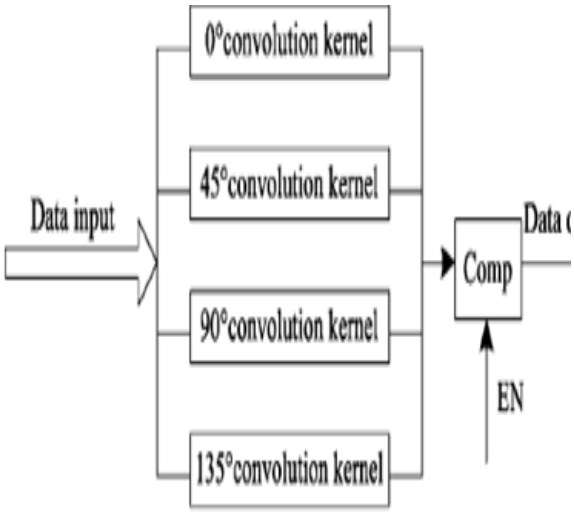


Fig 2.4 Sobel Operator Parallel Structure.

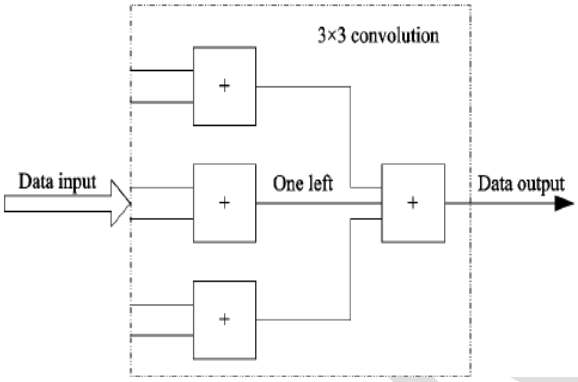


Fig 2.5 Convolution Structure.

3) Edges Control Module: The structure of edges control module is shown in Fig.4.6. Clk is the clock signal and Reset is the reset signal. Turn is enable signal when the Turn is valid the module works. EN is the output data control signal. This module can know where the current pixel location is and whether it is the edges of the image. Sobel edge detection enhancement operator can not deal with the left edge, right edge, the up edge and down edge. In this design the result of the edge pixels is set to zero otherwise call the Sobel enhancement operator module.

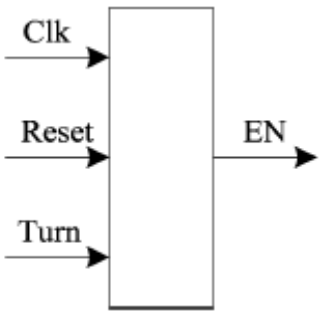
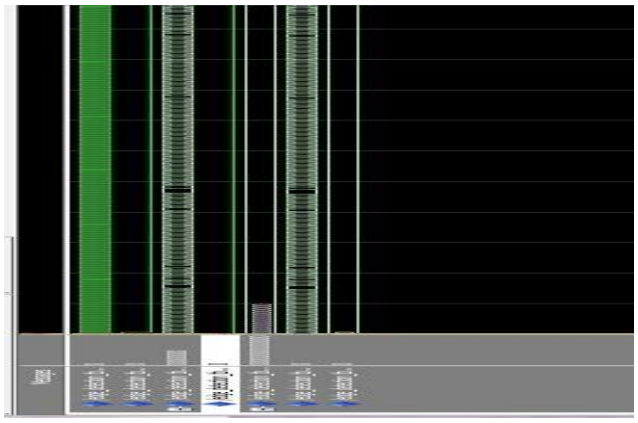


Fig 4.6 Edges Control Module.

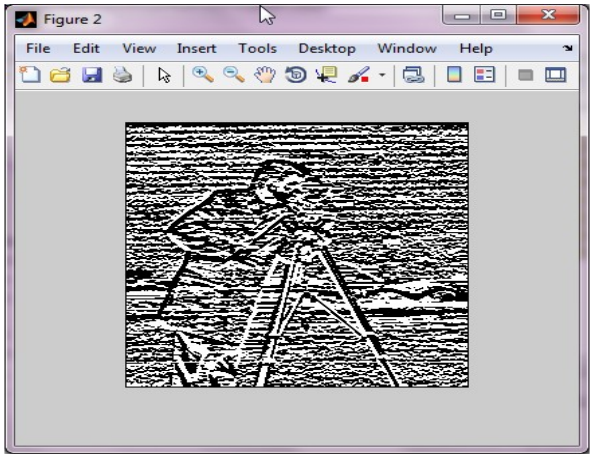
III. TESTING AND RESULTS

A. Simulation Results for Image Edge Detection.

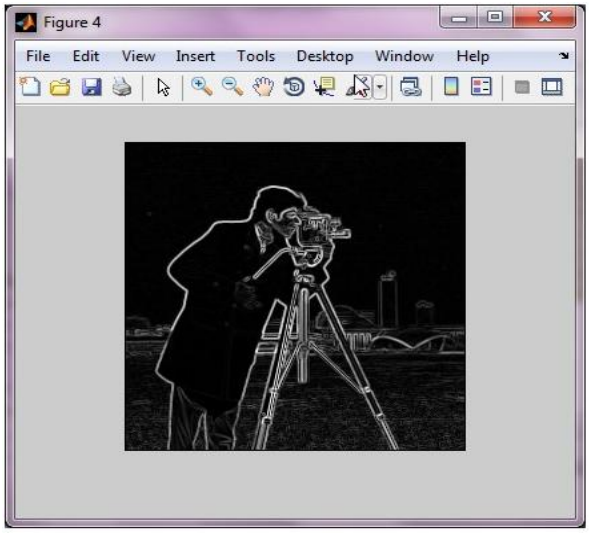


B. Original Image.

C. Gradient in X Direction

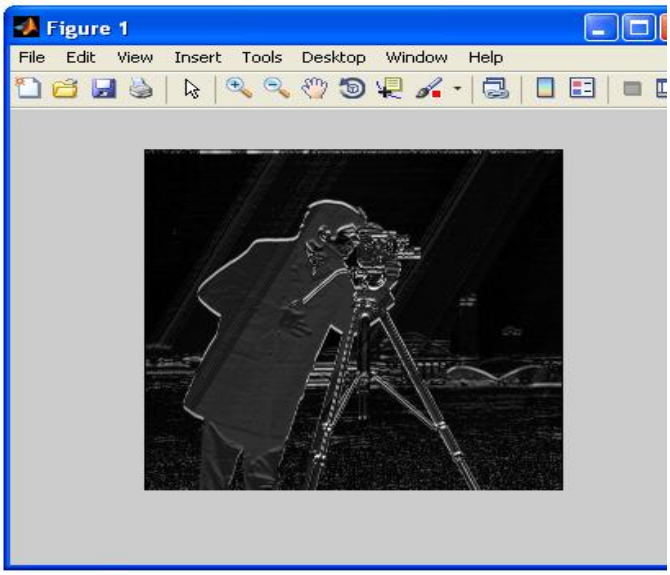


D. Gradient in Y Direction.



E. Edge Detection Using Matlab.

F. Output of VHDL Coding Using Edge Detection Module.



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