Various Digital Calibration Techniques in Pipeline ADCs (Analog to Digital Converter): A Theoretical Review

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***Abstract*-Analog-to-digital converters (ADCs) are key style blocks in analog electronics and are presently adopted in several application fields to enhance digital systems, which accomplish superior performances with relation to analog solutions. Application like wireless communication and digital audio and video have created the necessity for price effective information converters that may accomplish higher speed and backbone. varied samples of ADCs applications are often found in information acquisition systems, measure systems and data communication systems conjointly imaging, instrumentation systems. the subsequent article takes the data of options and demerits of the pipeline ADCs design and compares its options with four of the foremost fashionable architectures that are: flash, dual-slope, sigma-delta, ANd sequential approximation analog-to-digital converters (ADCs) conjointly enclosed an in-depth review of the operation, features, and advantages of pipeline design. this text concludes with a style of background standardisation technique in pipeline ADCs……..**

Keywords: flash, dual-slope, sigma-delta, and successive approximation analog-to-digital converters (ADCs), pipeline ADCs,DNL,INL,DAC.

I.INTRODUCTION

An analog-to-digital converter (ADC) is the most important component in analog and digital electronics, communication and video system. It acts as a bridge between the analog and digital worlds. It is a necessary component whenever data from the analog domain, through sensors or transducers, should be digitally processed or when transmitting data between chips through either longrange wireless radio links or highspeed transmission between chips on the same printed circuit board or different printed circuit boards.

With development of theseelectronics system, high resolution and high-speed ADCs are becoming more and more challenging. High-speed low-power Analog-to-Digital converters (ADCs) are the critical buildingblocks for modern communication and signal processing systems. Since the mid-1970s, ADCs have been widely designedusing integrating, successive approximation, flash, and delta-sigma techniques. At present,there a new class of ADC that is developed known aspipeline, which offered anattractive combination of high speed, high resolution, low power dissipation and small die size[1].

A. What is anADC Converter?

It is a device used to produce a digital output corresponding to the value of the signal applied to its input relative to a reference voltage.

$$DIGITALOUTPUTCODE = \frac{AnalogInput}{ReferenceInput} \times (2^N - 1)$$

The basic fundamentals processes in ADCs are:

- *Sampling*
- *Quantization*

The ADC Architectures are:

- *Flash Type ADCs*
- *Successive Approximation ADCs*
- *Integrating ADCs*
- *Sigma-Delta ADCs*
- *Pipeline ADCs*

1)Flash Type ADCs: This type is the fastest direct conversion, so better named as "flash" conversion also refers as parallel ADCs. It performsmultibit conversion directly. This type of converter utilizes the parallel differential comparators that compare reference voltages with the analog input voltage. As shown in fig 1, 2^N-1 comparators are connected in parallel each converter has N-bit resolution and the reference voltages is set by a resistor network[2].

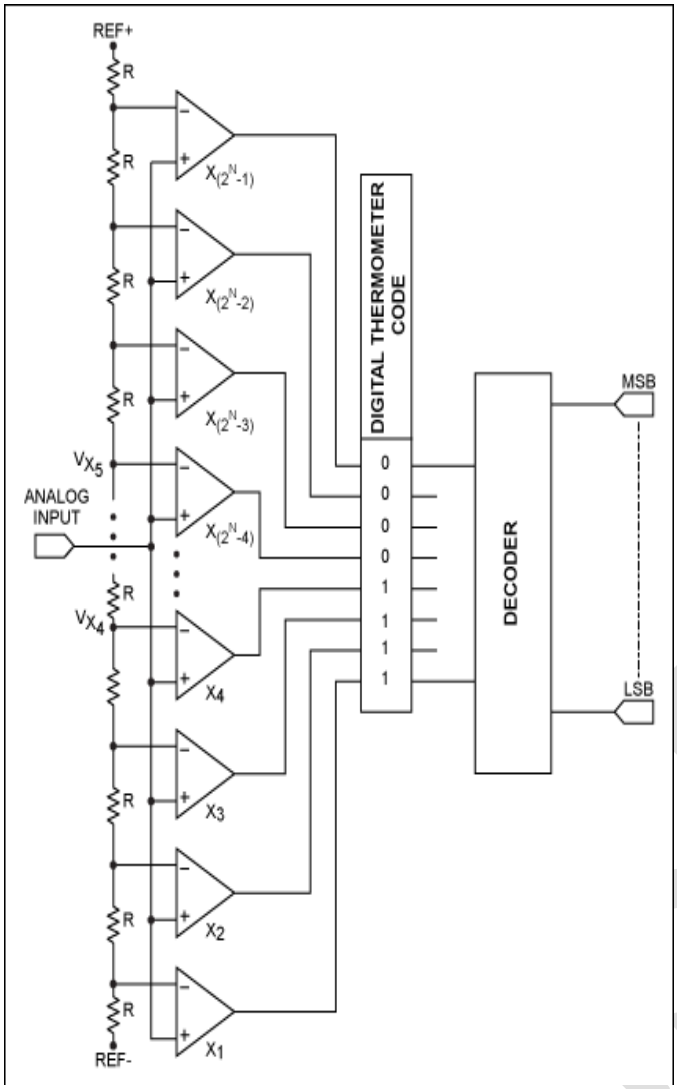

Fig. 1 Block diagram of Flash type ADCs

Flash ADCs are most applicable where very large bandwidths require. For high frequency applications likein satellite communication, data acquisition, sampling oscilloscopes, radar processing and high-density disk drives this type of ADCs is preferred.

2*) Successive-approximation ADCs:*Thistype of conversion is also known as bit-weighing conversion. SAR converters in their architecture have a single comparator, single DAC, a SAR, and a logic control unit. The system enables the MSB first, then the next significant bit, and so on. After all the bits of the DAC have been tried, the conversion cycle is complete. The processing of each bit takes one cycle; so the total conversion time for an N-bit SA-type ADC will be N clock cycle.

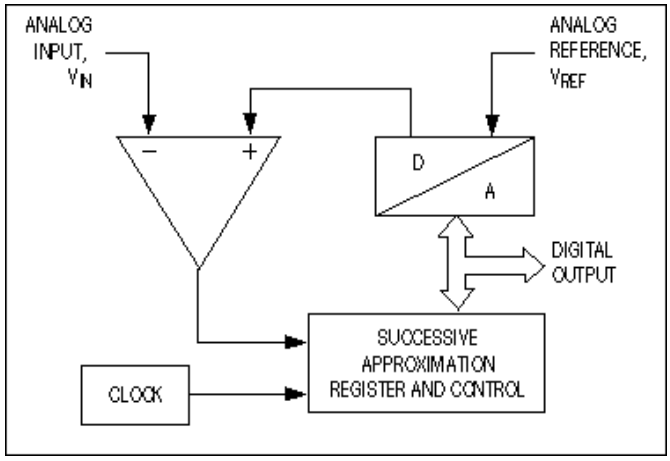

Fig. 2 Block diagram of SAR ADCs

It offers low supply current, and the lowest production cost, but the design is intensive and time consuming[1].

3) Integrating ADCs: Integrating ADCs this is also known as dual- or multi-slope data converters. It one of the slowest converters, but is relatively inexpensive because it does not require precious components such as DAC or VCO.

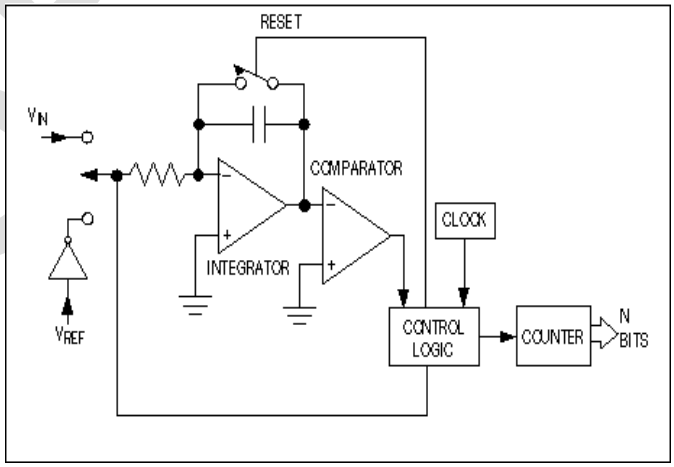

Fig. 3 Block diagram of Integrating ADCs

These are slow devices with low input bandwidth but still they are preferred for noisy industrial environments due to the ability of rejecting high-frequency noise and it can also fixed low frequencies like 50-60Hz. It's used in conversion in strain gauges and in thermocouple applications.

4) Sigma-Delta (Σ-Δ) ADCs: Sigma-delta (Σ-Δ) converters have relatively simple structures also known as oversampling converters. The architecture has a analog modulator followed by a digital decimation filter (Figure 4). This analog modulator blockhas an integrator and a comparator which consist a feedback loop of a 1-bit DAC. The DAC is used here as aswitch that just connects the input of comparator to the

reference voltage that may be positive or negative. It requires a clock unit for providing proper timing in the modulator and digital filter.

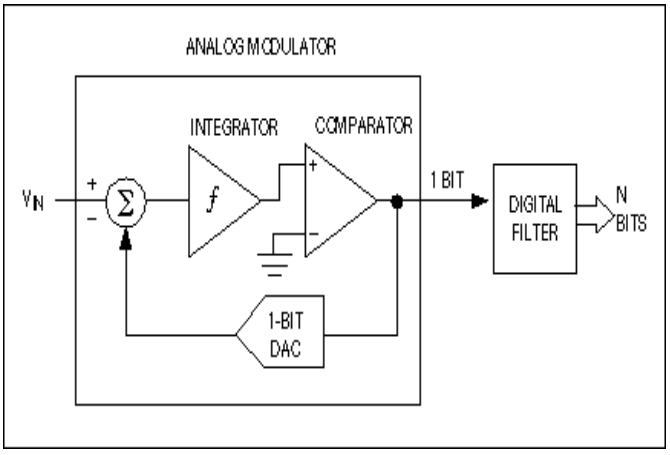

Fig. 4 Block diagram of Sigma-Delta ADCs

Low-bandwidth signals are applied to the input of this ADC which quantized with very low around 1-bit resolution and the sampling frequency is of 2MHz or larger.It is slower than pipeline ADCs and limited to lower input bandwidths, but the principle has developed a strong concept in the data-converter market. It is employing three major benefits:

- Having Low-cost with high-performance in conversion.
- Digital filter has the conversion circuitry.
- DSP-compatible for system integration.

B.Architectural Trade Off

The factors which decide the type of ADCs in various applications are following:

*a) Conversion time:*The time which is takenby ADCs to complete a conversion is called conversion time.The Graph between conversion time and number of bits of resolution for all types of converters is shown in Fig 5.

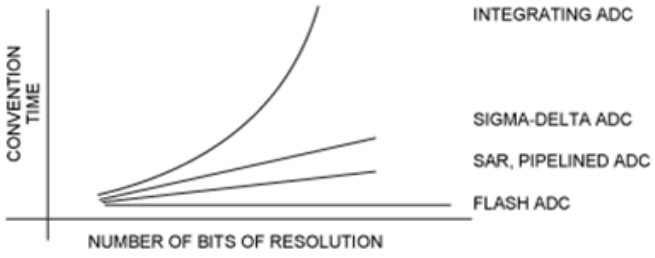

Fig. 5Graph between conversion time and number of bits of resolution

b) Component matching requirements in the circuit is second factor for choosing the ADCs for different applications shown in Fig. 6.

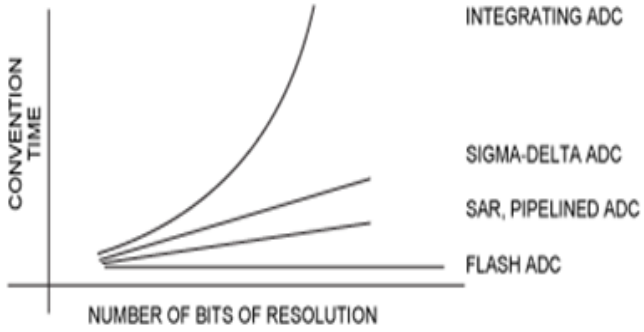

Fig. 6 Graph between component matching and number of bits of resolution

c) Die size, cost, and power. The graph between complexity and number of bits of resolution shown in fig 5c. It gives the result that if increases the die size cost increases with it.

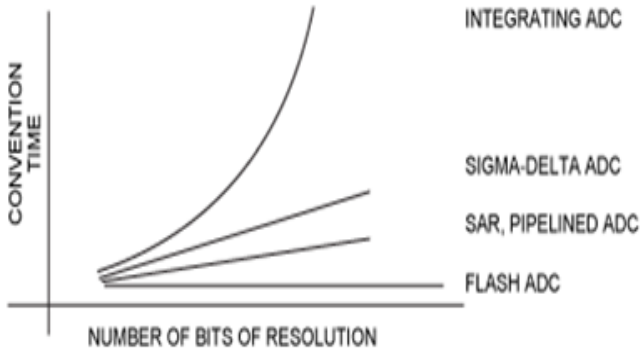

Fig. 7Graph between complexity and number of bits of resolution

C. Pipelined ADCs

Some applications in digital communication require high resolution, high speed and low power ADC. Pipeline ADC is better option for these kinds of applications because it may have resolution of 10-14 bits with sample rates more than 50 MSPS. Pipelined ADCs are widely used in the areas of wireless communications, digital subscriber line analog front ends, CCD imaging digitizers, studio cameras, ultrasound monitors and may other high speed applications.

But in pipeline ADC it is getting more and more challenging to increase resolution and speed with low power and high linearity. Some error are introduced in output of pipeline ADC due to capacitor mismatch, finite OPAMP gain, offset error etc which restrict high speed, resolution and low power. Calibrations techniques are used to remove the errors present output of pipeline ADC due to these factors and hence improve the performance pipeline ADC. So we can design high speed and low power pipeline ADC and if there is any nonlinearity or error is present in output then calibration block

is there to correct the output. Digital calibration techniques are preferred because it can be made as separate block, consumes less power and also no changes are needed in analog part of pipeline ADC due to which speed of pipeline ADC is not sacrificed.
The new pipeline architectures simplify ADCs design provide advantages as well:

- Extra bits at per stage with optimize correction in overlapping errors.
- Individual track-and-hold amplifiers for each stage gives each previous track-and-holdsample to process the next incoming one.
- Lower power consumption.
- Higher-speed conversion time is approx 100ns having less cost with less design time and effort.

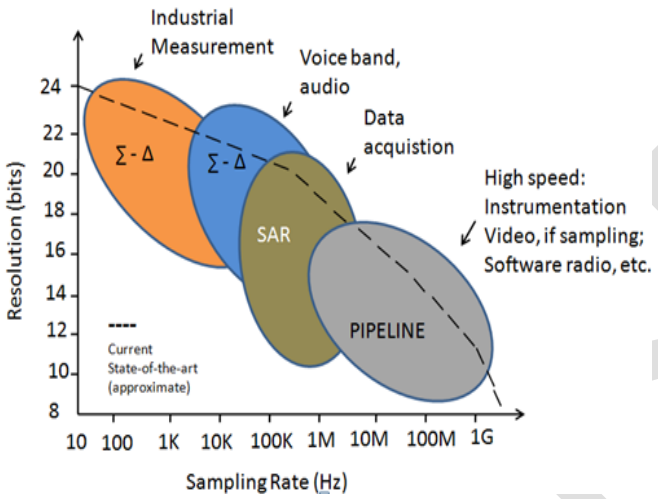

Fig. 8ADC architectures, applications, resolutions and sampling rates [16].

II.LITERATURE SURVEY

Lane Brooksand Hae-Seung Lee [2]presented a method of indirect background digital calibration of the dominant static nonlinearities in pipelined analog-to-digital converters. This is called decision boundary gap estimation (DBGE). It continuouslynotes the output ofADC to find the size of code gaps which result at the decision boundaries of each stage. Code gaps are resulted such effects as finite opamp gain, charge injection, capacitor mismatch, finite current source output impedance and comparator offset. It needs notadditional analog hardware or any specific calibration signal. The calibration is performed using the input signal and thus requires that the input signal exercise the codes in the decision boundaries at each stage. If it does not exercise this type of codes results the lack of calibration that is less critical due to the nonlinearities will not show in the output signal.

Andrea Panigadaand Ian Galton [3]presented in their paper that pipelined ADC conclude thetwo fully integrated digital background calibration techniques. The first one is known as harmonic distortion correction (HDC) used tocompensation in residue amplifier gain error and nonlinearity. The second one is called DAC noise cancellation (DNC) which is used for compensation in DAC capacitor mismatches. It is the first IC implementation of HDC, and the results demonstrate that HDC and DNC together facilitate low-voltage operation and enable reductions in power dissipation relative to the pipeline ADCs.

In the past decade, much of the research on analog-to-digital converters (ADCs) has focused on increasing speed, sampling rate and resolution.

Bob Verbruggen et al[4] presented four-way interleaved very fast ADC for communication in the unlicensed frequency band around 60GHz.

AshutoshVerma[5] has proposed an accurate resistor ladder topology for calibration in pipeline ADCs resultsop amp nonlinearity, remove residue gain error and DAC error. With high-speed and low-power op amp design, the Analog and digital converter gets 53 dB SNDR in the power consumption of 55 mW.

A 16-bit analog-to-digital converter designed in a complementary SiGeBiCMOS SOI process has been presented by
Robert Payne et al [6]. Although the designed ADC uses four-stage pipeline architecture, several techniques are incorporated to achieve 16 bits of distortion performance at a sample rate of up to 160 MHz. For better high input frequency linearity a T/H with a sampling instant modulation scheme is used.

A hybrid delta-sigma/pipelined modulator is presented by **OmidRajaee et al** [**8].** This proposed modulator gives the benefits of high resolution with distributed pipelined quantization, and combines this with the noise shaping property of a delta-sigma modulator. Its result is gain, swing, and slew requirements of the integrator are reduced. The modulator also makes use of the latency in the pipelined quantization to enhance noise shaping. This benefits less power dissipation with high stability and larger resolution.

Imran Ahmed [9]A low-power pipelined ADC topology is presented which uses capacitive charge pumps, source-followers, and digital calibration to eliminate the need for power-hungry opamps to achieve good linearity in a pipelined ADC.this is a technique to significantly reduce pipelined ADC power was discussed. Low power was achieved by using a simple architecture consisting of a charge pump combined with a source-follower and digital calibration, which replaced the functionality of power-hungry opamp based pipeline stages.

Yin Xiumei, Zhao Nan, SekediBomehKobenge, and Yang Huazhong [10]introduced a two-mode digital calibration technique for pipelined analog-to-digital converters (ADC). This calibration technique removes the errors of residual difference voltage generated by capacitor mismatch of pseudorandom sequence injection capacitors at the ADC initialization, while applies digital background calibration to continuously compensate the interstage gain errors in ADC normal operation. It not only decreases the complexity of analog circuit by eliminating the implementation of PN sequence with accurateamplitude in analog domain. But also improves the performance of digital background calibration by minimizing the sensitivity of calibration accuracy to sub-ADC errors. The use of opamps with low DC gains in normal operation makes the proposed design more compatible with future nanometer CMOS technology.

Sun Kexuand He Lenian [11]gives a fast combination calibration scheme of foreground and background. It is proposed so that the calibration parameter can be extracted immediately at startup by the foreground calibration and continuously updated rapidly to adapt to device and environment changes by background calibration, without interrupting normal ADC conversion. It takes 2688 conversions to complete the foreground calibration. A parallel background calibration with signal-shifted correlation is also proposed in this paper in order to reduce the background calibration tracking cycle.

1) Working of pipeline ADCs: Multi-stage pipeline ADCs are one of the most popular architecture for high speed application because it consists of low resolution flash ADC as its sub ADC in each stage. Also each stage contains a DAC and a subtractor, and residue gain amplifier as shown in fig 6. The last stage needs only a sub ADC. Sometime an additional S/H circuit is used at the input to avoid delay skew errors in two input signals to the subtractor. The total number of output codes of any stage depends on the resolutions of sub ADC used in that stage. If sub ADC used is say n bits, then total number of output codes will be 2^n.The working of pipeline ADC is explained in following steps:

1. First in input signal V_{IN} (i) is sampled using sample and hold amplifier (SHA) and then this sampled signal is converted into corresponding digital using sub ADC. That sub ADC is actually flash ADC. For n bits, this sub ADC will have 2^{n-1} comparator.

2. After getting digital output from sub ADC, we will get quantized analog signal as output of sub DAC. That quantized analog signal will be subtracted from original input signal. The difference of these two signals is known as residue voltage, V_{RES}.

3. The dynamic range of residue voltage will be $V_{REF}/2^k$. Where $V_{REF}$is full scale voltage range,To operate this signal on next stage, either we have to scale down the reference voltage or we have to convert residue voltage into full scale range, so that next stage can operate on residue signal. But scaling down the reference voltage for each stage with good accuracy is very difficult. Therefore we have to multiply it with gain of 2^k to convert signal into full scale range. Where k is resolution of that stage.

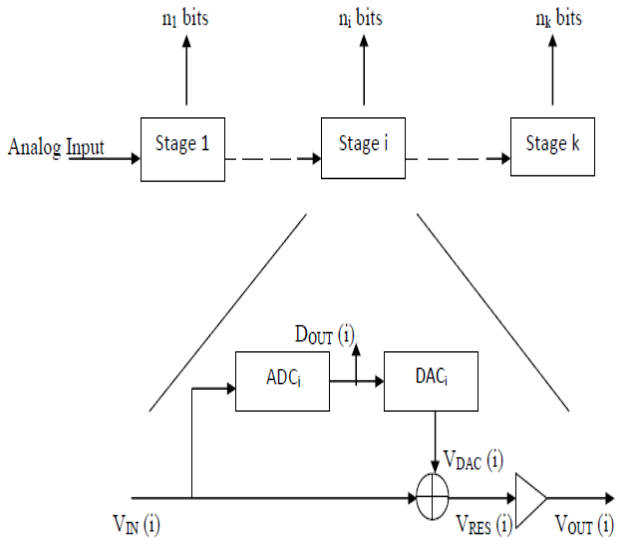

Fig. 9 Architecture of pipeline ADCs

4. So, now all stages of pipeline ADC will be identical. And sub DAC and residue amplifier together is known as multiplying DAC. This MDAC block consists of OPAMP which act as residue amplifier and speed of OPAMP normally limit the performance of pipeline ADCs.

5. After amplifying the signal, it will be input to next stage. And this way, the processing will take place. So there will be some delay between the outputs of each stage.And we have to align and synchronize the output bits of each stage to get final output.

In pipeline ADC, last stage does not require any further processing. So in last stage we require only flash ADC of resolution of k bits. And also if each stage of pipeline ADC has k bit resolution and total number of stages is n, then total resolution of pipeline ADC will be n × k.

SYSTEM ARTITECTURE	RESOLUTION	SPEED	ADVANTAGES/DRAWBACKS
Flash	8 bits	250 Msps-1Gsps	+ Extremely fast + High input bandwidth – Expensive – High input capacitance – High power consumption – Large die size
SAR	10 bits-16 bits	76 ksps-250 ksps	+ High resolution and accuracy + Low power consumption + Few external component – Low input bandwidth – Limited sampling rate – V_{in}must remain constant during conversion
Integrating	>16 bits	<50 ksps	+ High resolution + Low supply current + Excellent noise rejection – Low speed
Sigma-Delta	>16 bits	> 200 ksps	+ High resolution + High input bandwidth + Digital on-chip filtering – External T/H – Limited sampling rate
Pipeline	12 bits- 16 bits	1Msps-80Msps	+ High throughput rate + Low power consumption + Digital error correction and on-chip self calibration – Requires 50% duty cycle typical – Requires minimum clock frequency

Table 1) Comparisons between different types of ADCs

CONCLUSION

Here we have seen that in digital calibration block separate digital architecture is used and no modification in architecture of pipeline ADC is required than analog calibration technique. We also studied the various background digital calibration techniques. These digital calibration techniques can really enhance the performance of pipeline ADC. These techniques are very useful in those applications area where high accuracy is required.These proposed algorithms are that they uses sinusoidal signal for calibration. This algorithm [13] is working in presence of noise also. So, not accurate sinusoidal signal is required for calibration which can be generated easily.We will introduce a digital calibration technique for pipeline ADC which can remove the error present in the output of pipeline ADC due to capacitor mismatch, finite OPAMP gain and change of comparator threshold level.

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