

High Efficiency Single-stage Grid-tied PV Inverter Topology for Renewable Energy System

Prof. S. S. Patil

*Dept. of Electronics and Telecommunication Engineering
STES's Sinhgad Institute of Technology
Lonavala, University of Pune, India
sulakshana1087@rediffmail.com*

G. S. Patil

*Dept. of Electronics and Telecommunication Engineering
STES's Sinhgad Institute of Technology
Lonavala, University of Pune, India
optimalgopalpatil@gmail.com*

Abstract—This paper Proposed Single Stage High Efficiency which has a high performance Boost-Buck Converter Based on single-stage inverter topology for grid connected photovoltaic (PV) systems for the renewable energy system. The energy storage needs to be at the front of a single stage inverter, and it is usually implemented by electrolytic capacitors. The lifetime issue of an electrolytic capacitor is introduced. And the conclusion can be drawn that although the electrolytic capacitors have limited lifetime, it can still be used by applying smaller voltage and current ripple to prolong its lifetime. Because the end of its life doesn't mean it failed, the electrolytic capacitor can work much longer than its estimated lifetime. As the capacitance also has an impact on maximum power point tracking (MPPT) efficiency, the larger capacitance leads to higher MPPT efficiency. After that, a boost-buck converter based inverter is proposed. It operates in either boost or buck mode; thus, it has a wide input voltage range or high efficiency can be achieved. Then, the analysis of its middle capacitor and continuous current mode/discontinuous current mode (CCM/DCM) operation condition is presented. Since the common-mode voltage in this inverter is equal to the grid voltage, it changes at line frequency. Thus, the leakage current of it is very small even at an extreme case.

Keywords— photovoltaic (PV), MPPT, CCM/DCM, Boost-Buck converter, capacitance.

I. INTRODUCTION

With rising fuel costs, increasing concerns for global climate change, and a growing worldwide demand for electricity, utilizing renewable energy sources such as solar power becomes a necessity rather than a luxury. The total solar energy absorbed by Earth's atmosphere, oceans and landmasses is approximately 3,850,000 exajoules (EJ) per year but only a fraction of that is captured for electrical power production. Solar powered systems can generate electricity using photovoltaic (PV) panels, or thermal collectors. The world solar PV market installation reached a record high of 5.95 gigawatts (GW) in 2008.

A single-phase grid connected transformer less photovoltaic (PV) inverter for residential application is presented. The inverter is derived from a boost cascaded with buck converter along with a line frequency unfolding circuit. Due

to its novel operating modes, high efficiency can be achieved because there is only one switch operating at high frequency at a time, and the converter allows the use of power MOSFET and ultra-fast reverse recovery diode. This dissertation begins with theoretical analysis and modelling of this boost-buck converter based inverter. And the model indicates small boost inductance will leads to increase the resonant pole frequency and decrease the peak of Q, which help the system be controlled easier and more stable. Thus, interleaved multiple phase's structure is proposed to have small equivalent inductance, meanwhile the ripple can be decreased, and the inductor size can be reduced as well. A two-phase interleaved inverter is then designed accordingly. The double-carrier modulation method is proposed based on the inverter's operation mode. The duty cycle for buck switch is always one if the inverter is running in boost mode. And the duty cycle for boost switches are always zero if the inverter is running in buck mode. Because of this, the carrier for boost mode is stacked on the top of the carrier for buck mode, as a result, there is no need to compare the input and output voltage to decide which mode the inverter should operate in. And the inverter operates smoothly between these two modes.

The second part of the paper deals with the type of topologies that have been implemented with their advantages and the drawbacks. The third part of the paper deals with charging capacity of the proposed configuration. The fourth part deals with the detailed description of the proposed topology and gives the experimental results in Matlab .The fifth part deals with the design of the passive components used in the inverter topology. The sixth part deals with the comparison of all the proposed configurations on the basis of simulation and experimental results. The seventh part deals with leakage current analysis and the last part deals with the conclusion and references.

II. SINGLE STAGE PV INVERTER

A. State-of-the-art Single Stage PV Inverters

Here, single stage inverter is defined as an inverter with one stage of high frequency power processing. That means it has only one high switching frequency stage. Figure 1.1 through

Figure 1.3 shows the state-of-the-art single stage PV inverters.

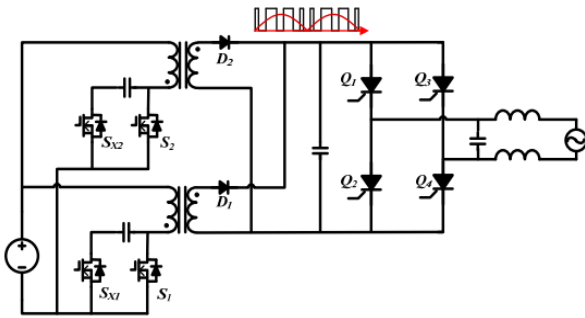


Figure 1.1 Emphases micro-inverter

In Figure 1.1, the interleaved flyback converters serve as single-stage power conversion. Sx1 and Sx2 are auxiliary switches for active snubber. Q1, Q2, Q3, and Q4 are thyristor, which serve as polarity selection switches.

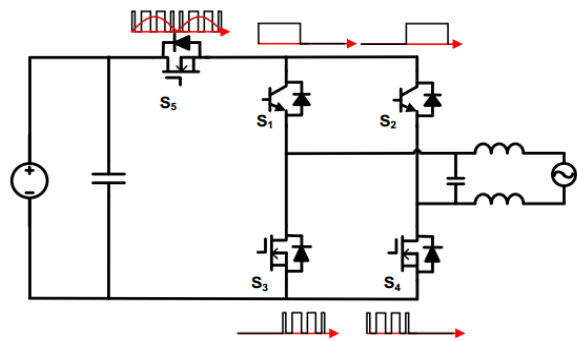


Figure 1.2 SMA H5TM inverter

In Figure 1.2, buck switch S5 produces rectified SPWM. IGBT's S1 and S2 serve as low frequency selection network. MOSFET S3 operates in SPWM on negative cycle. MOSFET S4 operates in SPWM on positive cycle. Use fast recovery diode for S1 and S2 to reduce reverse recovery loss. S5 and S3 or S4 share half the DC bus voltage, allowing Low-voltage switches to be used in high voltage input. Other than high efficiency, the most advantage of this inverter is it has no leakage current, which is important for PV application. The drawback of this inverter is that the input voltage of it should be higher than the peak of the grid voltage, which limits the input voltage range for a PV inverter.

B. (HERIC) inverter

Similar as H5TM's concept, the diagonal switches (S1 – S4) and (S2 – S3) pairs switch alternatively during positive and negative line cycles. Auxiliary switches (S5 and S6) turn on during zero states or freewheeling period and turn off during powering states, so only the auxiliary diodes need to be ultrafast reverse recovery, but the main diodes can be slow one. It should have even higher efficiency than H5TM because of only two switches in series during on time

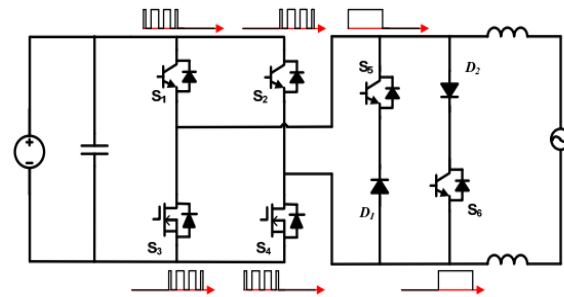


Figure 1.3 Highly efficient and reliable concept (HERIC) inverter

And it doesn't introduce leakage current either. For these single stage PV inverters, either a transformer is used for boosting the input voltage or the input voltage requires being higher than the peak of the grid voltage, which is not good for PV application because the PV panel's I-V characteristics changes all the time [1][2].

III. ENERGY STORAGE IN SINGLE STAGE PV INVERTERS

A. Capacitance Calculation

Figure 2.1 illustrates the relationship between the input power and output power for a single phase PV inverter. Because of the power difference, the single phase inverters always need energy storage to balance the instantaneous energy between input and output. Since single stage inverter only has one power processing stage, this energy storage need to be placed in the front of the inverter as shown in Figure 2.2.

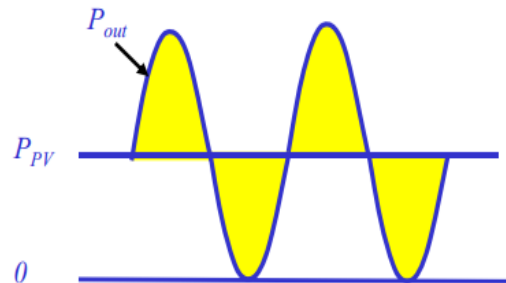


Figure 2.1 Input power and output power for a single phase PV inverter

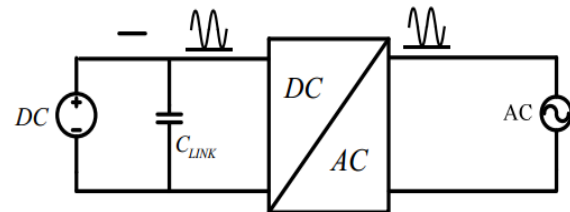


Figure 2.2 Single stage inverter

For a grid-tied PV inverter, it is required to have unity power factor by standards. In order to achieve unit power factor, the output current and voltage should have the same phase. Thus, the output power can be expressed as

$$P_{out}(t) = \sqrt{2}V_{grid} \cdot \sin(\omega_{grid} \cdot t) \cdot \sqrt{2} \frac{P_{PV}}{V_{grid}} \sin(\omega_{grid} \cdot t) \tag{1}$$

Where $P_{out}(t)$ is the instantaneous power; P_{PV} is the dc power from the input PV panels; V_{grid} is the grid's rms voltage. Thus, the output power could be simplified as

$$P_{out}(t) = 2P_{PV} \cdot \sin^2(\omega_{grid} \cdot t) = P_{PV} - P_{PV} \cdot \cos(2\omega_{grid} \cdot t) \tag{2}$$

Then the energy stored at the capacitor can be calculated as

$$\int [P_{out}(t) - P_{PV}] \cdot dt = \frac{1}{2} C \cdot u_{Cmax}^2 - \frac{1}{2} C \cdot u_{Cmin}^2 \tag{3}$$

Thus, the capacitance can be obtained as below

$$C = \frac{P_{PV}}{\omega_{grid} \cdot u_C \cdot \Delta u_C} \tag{4}$$

B. MPPT Efficiency

For the single stage PV inverter, the energy storage capacitors are required to keep the voltage out from the PV panels with small fluctuation in order to get maximum output power from the PV panels. Because of the voltage fluctuation, the power obtained from PV panel is also fluctuated [4]. The MPPT efficiency can be defined as

$$\eta_{MPPT} = \frac{\int_0^T P_{in}(t) dt}{T P_{MPP}} \tag{5}$$

The relationship between PV panels' current and voltage could be expressed as

$$U_{in} = U_{mpp} - \Delta u \cdot \cos(2\omega t)$$

$$\Delta u = \frac{P}{2\omega \cdot U_{mpp} \cdot C_{in}} \tag{6}$$

IV. PROPOSED BOOST-BUCK CONVERTER BASED PV INVERTER

A. Boost-Buck Converter Based PV Inverter Topology

A boost-buck type dc-dc converter is proposed as the first stage with regulated output inductor current, and a full-bridge unfolding circuit with 50- or 60-Hz line frequency is applied to the dc-ac stage, which will unfold the rectified sinusoid current regulated by the dc-ac stage into a pure sinusoidal current. Since the circuit runs either in boost or buck mode, its first stage can be very efficient if the low conduction voltage drop power MOSFET and ultra-fast reverse recovery diode are used. For the second stage, because the unfolding circuit only operates at the line frequency and switches at zero voltage and current, the switching loss can be omitted. The only loss is due to the conduction voltage drop, which can be minimized with the use of low on drop power devices, such as thyristor or slow-speed IGBT. In this version, IGBT is used in the unfolding circuit because it can be easily turned on and off with gating control. Since only the boost dc-dc converter or buck dc-dc converter operates with high Frequency switching all the time in the proposed system, the efficiency is improved. And because there is only one high frequency power processing stage in this complete PCS, the reliability can be greatly enhanced. Other than these, the analysis of middle capacitor and CCM/DCM operation condition is also presented [5][7].

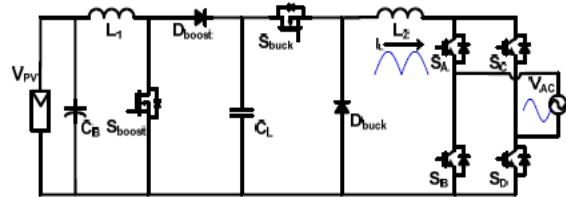


Figure 3.1 Boost-buck based PV inverter

B. Boost Mode

When the PV panel's voltage is lower than the instantaneous grid voltage, it will operate in boost mode, in which, S_{boost} will be switched on and off and S_{buck} will be always on, and the buck part of the circuit will act as an output filter as shown in Figure 3.2

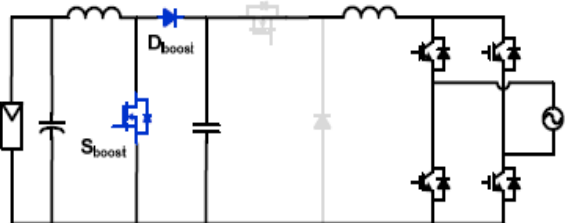


Figure 3.2 Boost Mode

In this mode, the duty cycle of S_{boost} can be found as

$$D_{boost} = 1 - \frac{V_{in}}{V_o}$$

Where $200 \leq 340 \leq V_{in}$ and $V_o = 340 \sin \omega t$, then it is easy to get

$$0 \leq D_{boost} \leq 1 - \frac{V_{in}}{340}$$

C. Buck Mode

When the PV panel's voltage is higher than the instantaneous grid voltage, it will operate in buck mode, in which, S_{buck} will be switched on and off and S_{boost} will be always off, and the boost part of the circuit will act as an input filter as shown in Figure 3.3

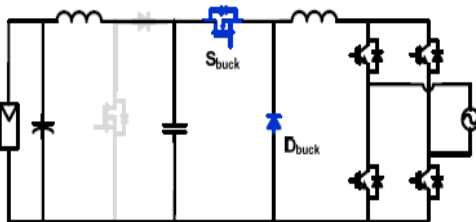


Figure 3.3 Buck mode.

In this mode, the duty cycle of S_{buck} can be found as

$$D_{buck} = \frac{V_o}{V_{in}}$$

Where $200 \leq V_{in} \leq 500$ and $V_o \leq 340 \sin \omega t$, then it is easy to get

If $340 \leq V_{in} \leq 500$ then

$$0 \leq D_{buck} \leq \frac{340}{V_{in}}$$

If $200 \leq V_{in} \leq 340$ then

$$0 \leq D_{buck} \leq 1$$

Thus, if the PV panel's voltage is lower than the grid's peak voltage, the PV inverter will switch between buck modes and boost mode depending on the instantaneous grid voltage as shown in Figure below. However, if the PV panel's voltage is higher than the grid's peak voltage, it will always run at buck mode. Instead of a dc bus in the middle, the voltage across the capacitor CL in boost/buck PV inverter varies with the grid, if PV panel's voltage is lower than the grid's peak voltage as shown in Figure 4.1. However, if PV panel's voltage is higher than grid's peak voltage, CL 's voltage will be the same as PV panel's voltage.

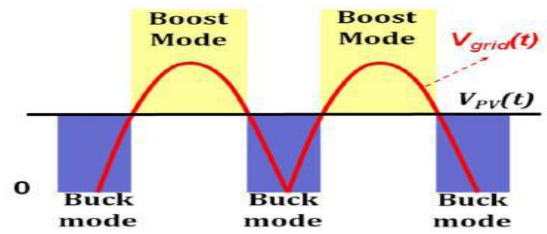


Figure 4.1 Operation mode.

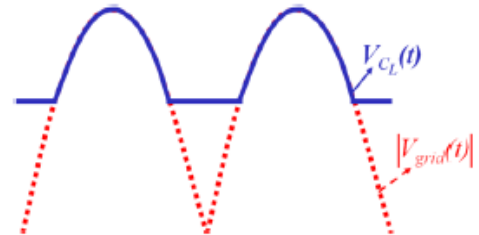


Figure 4.2 Capacitor CL's voltage.

V. PASSIVE COMPONENTS DESIGN

A. Capacitor Design

Based on the energy storage the input capacitance could be calculated as

$$C_B = \frac{P_{PV}}{\omega_{grid} \cdot U_C \cdot \Delta u_C} = \frac{2500}{2\pi \cdot 60 \cdot 200 \cdot 16} \approx 2000\mu F \tag{7}$$

The middle capacitor CL impacts Q factor and double-pole frequency. Large CL leads to small Q but low frequency double-pole, which is analyzed in 7 And also from the power decoupling point of view, as shown in Figure 4.2, large CL also leads to large Pulsating input power that means large C_{in} is needed to decouple the power, which is not expected. In our case 2 where F is chosen for CL .

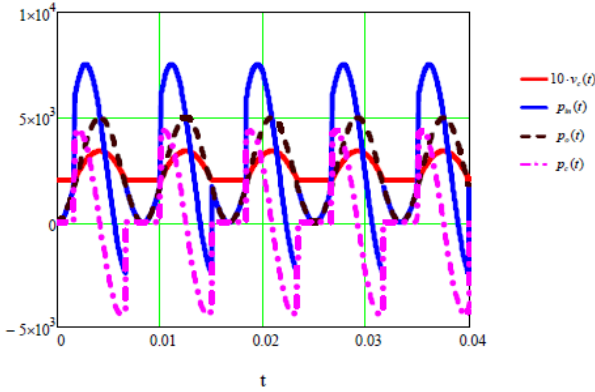
$$P_o(t) = v_o(t) \cdot i_{L_2}(t) = V_o \sin \omega t \cdot I_{L_2} \sin \omega t = V_o \cdot I_{L_2} \frac{1 - \cos 2\omega t}{2} \tag{8}$$

$$p_r(t) = C_L \frac{dv_c(t)}{dt} \cdot v_c(t) = \begin{cases} C_L \frac{d \left(V_o \sqrt{\frac{1 - \cos 2\omega t}{2}} \right)}{dt} \cdot V_o \sqrt{\frac{1 - \cos 2\omega t}{2}} & \text{if } V_{PV} < v_o(t) \\ C_L \frac{dV_{PV}}{dt} \cdot V_{PV} = 0 & \text{if } V_{PV} > v_o(t) \end{cases}$$

$$p_n(t) = p_r(t) + p_o(t) = \begin{cases} C_L \frac{d \left(V_o \sqrt{\frac{1 - \cos 2\omega t}{2}} \right)}{dt} \cdot V_o \sqrt{\frac{1 - \cos 2\omega t}{2}} + V_o \cdot I_{L_2} \frac{1 - \cos 2\omega t}{2} & \text{if } V_{PV} < v_o(t) \\ V_o \cdot I_{L_2} \frac{1 - \cos 2\omega t}{2} & \text{if } V_{PV} > v_o(t) \end{cases} \tag{9}$$

Table 1 lists the summary of every passive components parameter.

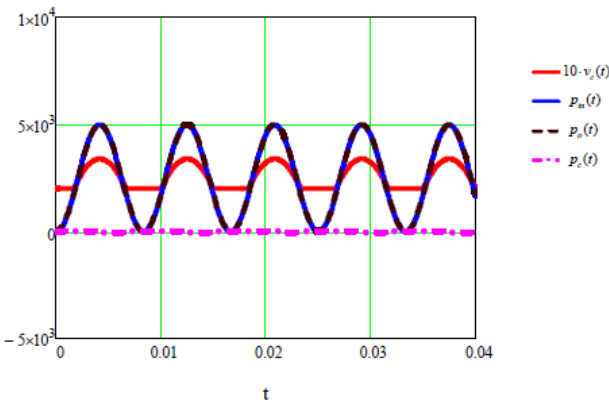
L_1	200 μH
L_2	400 μH
C_B	2 mF
C_L	2 μF



(a)

Figure 5.1 Pulsating power on input, output and C_L :

(a) $C_L = 200 \mu F$;



(b)

Figure 5.2 (b) $C_L = 2 \mu F$.

B. Inductor Design

During the buck mode, the input current can be treated as the input filter's inductor's current, whose ripple is much reduced from the filtering effect. Thus the input inductor is designed based on the current ripple in boost mode [4][5].

$$\Delta i_L = V_m \frac{\Delta T}{L_1} = V_m \frac{T \left(1 - \frac{V_o}{V_m}\right)}{L_1} = \frac{T}{L_1} \left(1 - \frac{V_o}{V_m}\right) V_m \tag{10}$$

And

$$\Delta i_{L2max} = 125 \cdot \frac{T}{L_2} \tag{11}$$

Thus

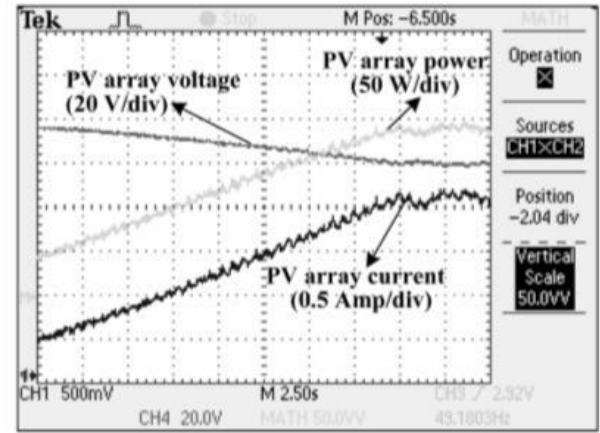


Figure 6.1 Boundary scan condition for the traditional hill climbing method.

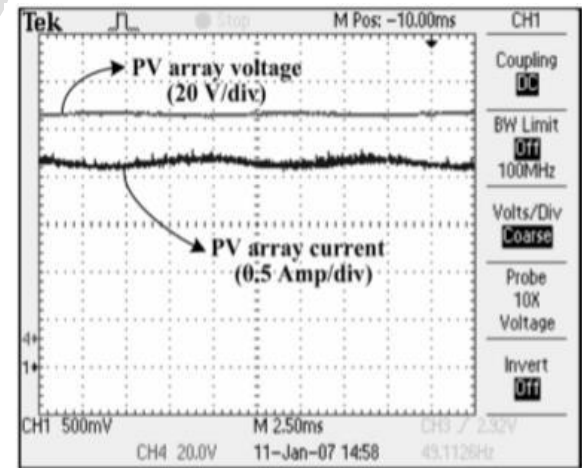


Figure 6.2 Boundary power condition for output current with different input voltage.

As mentioned before, during the buck mode, the input current can be treated as the input filter's inductor's current, whose ripple is much reduced from the filtering effect. Similarly, during the boost mode, the output current can be treated as the output filters Inductor's current, whose ripple is also much mitigated. Due to this dual filter effect, the DCM mode operation is very rare in the proposed circuit.

In fact, the circuit is always running in continuous current mode (CCM) for input current in buck mode and output current in boost mode [8]. That also indicates that discontinuous current mode (DCM) or boundary mode can happen only in output current in buck mode and input current in boost mode. Then it can be analyzed as a normal buck and boost converter. The boundary condition can be derived based on the input current ripple for boost mode and output current ripple for buck mode as below

$$\Delta I_{in} = \frac{1}{2} \cdot \frac{\Delta T}{L} \cdot V = \frac{1}{2} \cdot \frac{1}{f_{sw}} \cdot \left(1 - \frac{V_{in}}{V_o}\right) \cdot V_{in} = \frac{1}{20} \cdot \frac{V_{in} \cdot V_o - V_{in}^2}{V_o}$$

$$\Delta I_o = \frac{\Delta T}{L} \cdot V = \frac{1}{f_{sw}} \cdot \left(1 - \frac{V_o}{V_{in}}\right) \cdot V_o = \frac{1}{20} \cdot \frac{V_{in} \cdot V_o - V_o^2}{V_{in}}$$

(12)

Based on the equations above, it is easy to derive that the maximum ripple of input current happens when $V_{in} = 200$ V and $V_o = 340$ then $\Delta I_{inmax} = 4.12$ A. And the maximum ripple of output current happens when $V_{in} = 500$ V and $V_o = 250$ V then $\Delta I_{oinmax} = 6.25$ A. Thus, the boundary power for different input voltage can be obtained shown in figure below (figure 6.1 and 6.2)

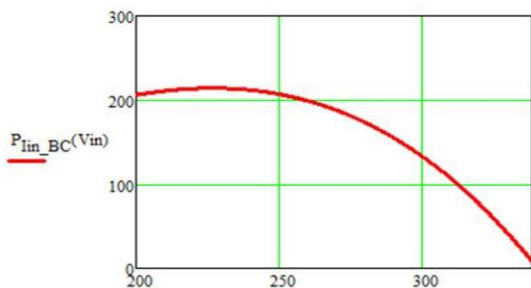


Figure 6.3 Boundary power condition for input current with different input voltage.

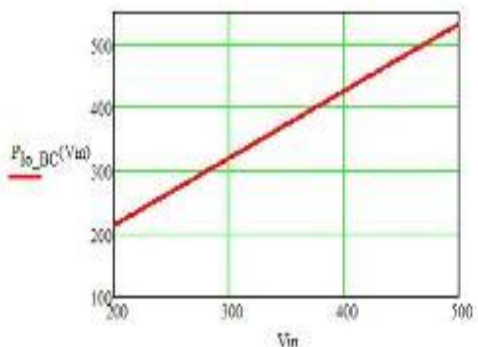


Figure 6.4 Boundary power condition for output current with different input voltage.

It is obviously noticed from Figure 6.1 and Figure 6.2 that the input current will go to DCM at very light power

condition, which is even lower than 10% of the rated power. And the output current will go to DCM at light power condition as well, which is 39 lower than 20% of the rated power at most of the input voltage. If DCM is not desired burst mode can be implemented at light power condition [9].

Table 2 lists the comparison of traditional hill climbing method and proposed Buck boost converter

Single Stage PV Inverters	SMA H5TM inverter	Proposed configuration buck and boost type inverter
The drawback of this inverter is that the input voltage of it should be higher than the peak of the grid voltage, which limits the input voltage range for a PV inverter.	For these single stage PV inverters, either a transformer is used for boosting the input voltage or the input voltage requires being higher than the peak of the grid voltage, which is not good for PV application because the PV panel's I-V characteristics changes all the time	The first converter art operates in either boost or buck mode, which offers a wide input voltage range and presents a big advantage in PV inverter applications

VII. LEAKAGE CURRENT ANALYSIS

It has reported that the capacitance between the point of contact and a single PV module has been calculated to range between 100 – 400 pF. The capacitance depends on weather conditions, and in the worst case as rainy days, the capacitance can be as high as 80 nF/kW. Because of there is no isolation between the input and output without a transformer, the transformerless inverter needs to consider the leakage current issue as shown in Figure 7.1. The maximum current which can flow through the human body is 0.2 mA. And the German standard lists the disconnection time for different levels of leakage currents as shown in Table 1. Figures and tables must be centered in the column. Large figures and tables may span across both columns. Any table or figure that takes up more than 1 column width must be positioned either at the top or at the bottom of the page. Graphics may be full colour. All colours will be retained on the CDROM. Graphics must not use stipple fill patterns because they may not be reproduced properly [7]. Please use only SOLID FILL colours which contrast well both on screen and on a black-and-white hardcopy, as shown in Figure 7.2

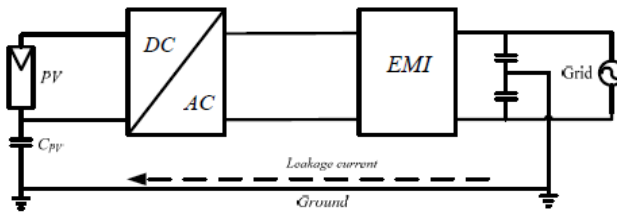


Figure 7.1 Leakage current in a PV transformer less grid-tied inverter system.

Table 3 Leakage current and corresponding disconnection time

RMS value of the leakage current (mA)	Disconnection time (s)
30	0.3
60	0.15
150	0.04

Because of this safety issue, the leakage current should be as small as possible for transformerless inverter. Many literatures analyzed the leakage current in transformerless grid-connected inverter. For the proposed topology, the negative terminal “O” of solar modules is set as the reference point, and the middle points of the bridge legs are set as “P” and “N” for the output terminals as shown in Figure

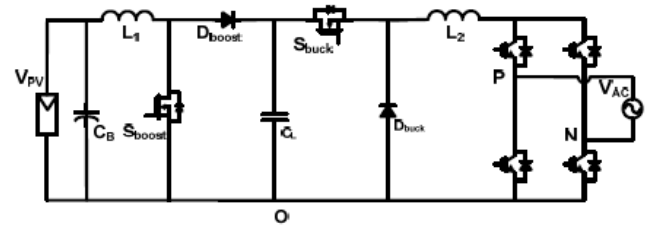


Figure 7.2 Boost-buck based PV inverter

Then the instantaneous common-mode voltage *v_{cm}* can be calculated as

$$v_{cm} = \frac{(v_{PO} + v_{NO})}{2} \tag{13}$$

If *v_{cm}* is keeping constant all the time, the leakage current could be avoided. For the proposed inverter, can be obtained

$$\begin{cases} v_{PO} = v_{grid} & v_{NO} = 0 & \text{if } v_{grid} > 0 \\ v_{PO} = 0 & v_{NO} = -v_{grid} & \text{if } v_{grid} < 0 \end{cases} \tag{14}$$

Thus

$$v_{cm} = \frac{|v_{grid}|}{2} \tag{15}$$

Since *v_{grid}* is not constant but sinusoidal with 60 Hz, there is a small line frequency leakage current in the proposed inverter. For a 2.5 kW system, the capacitance between the PV modules and the ground *C_{PV}* would as high as 200 nF. The simulated leakage current in this extreme case is shown in Figure 7.2. It shows that even in this extreme case, the leakage current is still far below the standard [8].

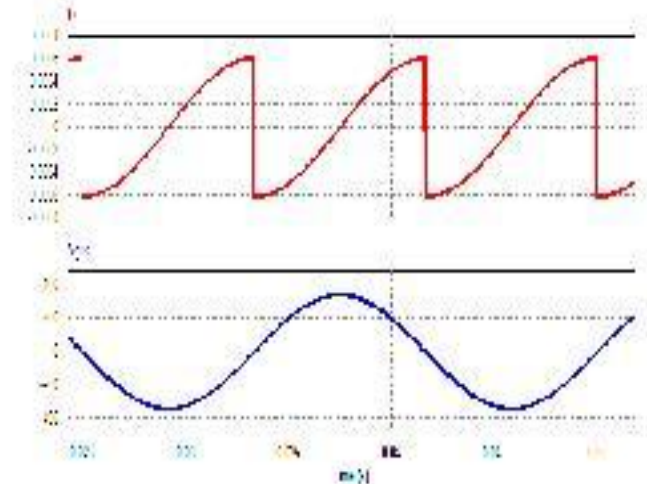


Figure 7.3 Leakage current with CPV = 200 nF.

VIII. CONCLUSION

In this paper, the state-of-the-art single stage PV inverters are reviewed firstly. For these single stage PV inverters, either a transformer is used for boosting the input voltage or the input voltage requires being higher than the peak of the grid voltage, which is not good for PV application because the PV panel's I-V characteristics changes all the time. Moreover, the capacitance also has an impact on MPPT efficiency. The larger capacitance leads to higher MPPT efficiency. After that a novel boost-buck converter based inverter has been presented. The first converter part operates in either boost or buck mode, which offers a wide input voltage range and presents a big advantage in PV inverter applications. Due all these process power either as a buck converter or a boost converter, high efficiency can be achieved.

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