Analysis of Leakage Power Reduction in 2-Bit Full Carry Adder using Power Gating

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***Abstract*- Adder circuits are basic and very important circuits in electronics. These form a base for many complex calculations in various electronic circuits. With the emerging technologies in electronics, there is a continuously increasing demand of the portable and compact devices with maximum battery life. VLSI and ULSI are thus significant technologies today. Many components can now be mounted on a single chip which has minimized the chip size. VLSI designing has many advantages like compact size of the device, portability, modularity etc, with an added disadvantage of leakage power dissipation.**

Thus, while developing VLSI chips, manufacturers have to constantly work upon various measures to reduce the leakage power dissipation. One method is to reduce the leakage current by raising the threshold voltage and lowering the supply voltage. Another method is power gating. In this approach, sleep transistors are used to disable entire blocks, when not in use.

In this technique, low leakage PMOS transistors are used as header switches to shut off the power supplies to those parts of the design which are in standby or sleep mode. Also, NMOS footer switches are used as sleep transistors.

Due to the insertion of the sleep transistors, the power network of the chip is now divided into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. Sleep transistors with high threshold voltage are used for power gating. This technique is Multi- Threshold CMOS (MTCMOS). The sizing of sleep transistor is an important constraint of designing. Power gating can be implemented using cell or cluster based (fine grain) approaches or a distributed coarse-grained approach.

In this paper, we will realize different approaches of reducing the leakage power in 2- bit full carry adder, by simulation methods using tanner tool.

I.INTRODUCTION

With rapidly increasing level of device integration and the rapid growth in complexity of electronic circuits, increased demand of portable electronics devices and also dependence on the battery operated devices is motivating the VLSI designers to reduce the power dissipation of the VLSI circuits so that they can be used for the long time for the given battery supply. the reduction of power is one of the pivotal parameter for designing of an efficient VLSI circuit. Also as high speed circuits dissipate large amounts of energy in a short amount of time, power minimization algorithm sand techniques are strongly suggested by most of the companies in these circuits. With ever increasing operating frequency and processing capacity per chip, large currents have to be delivered and the heat due to large power consumption must be mitigated by proper cooling techniques. Battery life in portable electronic devices is limited. Low power design directly leads to prolonged operation time in these portable devices. Besides this there are number of reason, for the motivation.

1. Reduction in device size
2. Growth of Modularity
3. Reliability
4. Low Power Target
4. Battery Life

II. PROPOSED DESIGN

The Proposed design uses the 2-bit full adder implementation of power gating at footer as well as header. i.e. there are two virtual nodes creates in the design one as virtual Vdd and another one as GND.

The basic strategy of power gating is to provide two power modes: a low power mode and an active mode. The goal is to switch between these modes at the appropriate time and in the appropriate manner to maximize power savings while minimizing the impact to performance.

The PMOS and NMOS Transistors used as header and footer are high **Vt** transistors as compared to other transistors in the circuit.

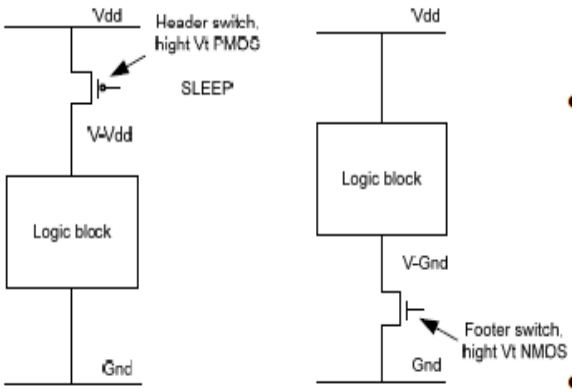

Fig.1 Power Gating Logic

A. Sleep transistors

1. Insert high Vt MOSFET between power rail and logic blocks
2. Header transistor off lead to logic block floating to near zero
3. Footer transistor off lead to logic block floating to near 1

The power gating technique is inculcated in the proposed full adder in such a way that it'll make the when the module is off, it operates on high **Vt** and when the circuit is on it operates on low **Vt.**

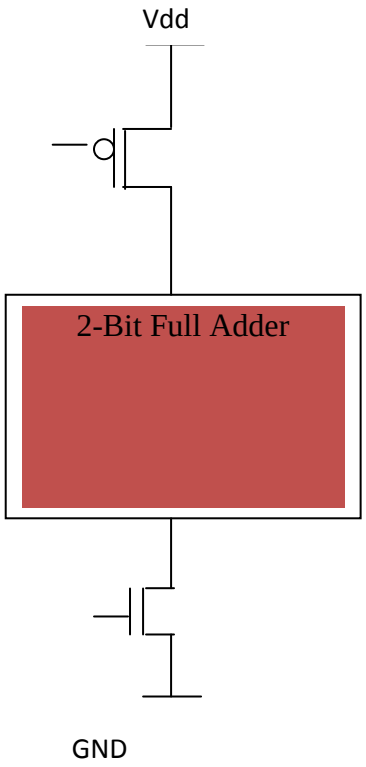

Fig. 2-bit Full Adder with Header

CONCLUSION

In our proposed design i.e. 2-bit full adder is intent to reduce the power consumption with the insertion of high **Vt** NMOS as well as PMOS transistors namely header and footer.

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