Power Dissipation of Combinational Circuits By Adiabatic Technique for 180nm CMOS Technology

Kapil Mangla[1] and Neha Mangla[2]
[1,2]*Department of Electronics and Communication Engineering, SCET Palwal, (HR)*
[1]Kapild@satyaedu.org, [2] nehamangla03@gmail.com

Abstract- This paper focuses on the importance of providing new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies. In this paper, various sources of power dissipation in modern VLSI circuits along with various power reduction techniques as adopted in industry today are discussed. The simulation has been carried out with properly defined simulation runs on a SPICE environment using a 0.18µm process. This thesis investigates one of the major sources of the power dissipation and proposes and evaluates the techniques to reduce the dissipation.

Keywords- CMOS Circuit, VLSI, Combinational Circuits, SPICE, Power.

I. INTRODUCTION

In the past few decades ago, the electronics industry has been experiencing an unprecedented spurt in growth, thanks to the use of integrated circuits in computing, telecommunications and consumer electronics. The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems. Higher power and energy dissipation in high performance systems require more expensive packaging and cooling technologies, increase cost, and decrease system reliability [1].

Digital CMOS integrated circuits have been the driving force behind VLSI for high performance computing and other applications, related to science and technology. The demand for digital CMOS integrated circuits will continue to increase in the near future, due to its important salient features like low power, reliable performance and improvements in the processing technology [4].

The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this thesis Work, a new CMOS logic family called ADIABATIC LOGIC, based on the adiabatic switching principle is presented[B].The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very Low power dissipation. Another technique called Conventional technique illustrate more power dissipation is been achieved by adiabatic Technique [2]. This thesis work demonstrates the low power dissipation of Adiabatic Logic by presenting the results of designing various design/ cell units employing Adiabatic Logic circuit techniques. A family of full-custom conventional CMOS Logic, an Adiabatic Logic for example a 2:1 MULTIPLEXER,HALF ADDER, FULL ADDER,HALF SUBTRACTOR and COMPARATOR are designed using 180 nm Technology.

II. STUDY AND ANALYSIS OF LOW POWER ADIABATIC COMBINATIONAL CIRCUITS

The popularity of complementary MOS technology can be mainly attributed to inherently lower power dissipation and high levels of integration. However, the current trend towards ultra low-power has made researchers search for techniques to recover/ recycle energy from the circuits. In the early days, researchers largely focused on the possibility of having physical machines that consume almost zero energy while computing and tried to find the lower bound of energy Consumption in conventional level-restoring CMOS logic circuits with rail-to-rail output voltage swing, each switching event causes an energy transfer from the power supply to the output node or from the output node to the ground.

During a 0-to-V_{DD} transition of the output, the total output charge

$Q = C_{LOAD} V_{DD}$ …(1)

is drawn from the power supply at a constant voltage. Thus, an energy of

$E_{SUPPLY} = C_{LOAD} V_{DD2}$ ...(2)

is drawn from the power supply during this transition. Charging the output node capacitance to the voltage level VDD means that at the end of the transition, the amount of stored energy in the Output node is:

ESTORED = CLOAD VDD2 / 2. …(3)

Thus, half of the injected energy from the power supply is dissipated in the PMOS network while only one half is delivered to the output node[3]. During a subsequent VDD -to- 0 transition of the output node, no charge is drawn from the power supply and the energy stored in the load capacitance is dissipated in the NMOS network.

To reduce the dissipation, the circuit designer can minimize the switching events, decrease the node capacitance, reduce the voltage swing, or apply a combination of these methods. Yet in all these cases, the energy drawn from the power supply is used only once before being dissipated. To increase the energy efficiency of the logic circuits, other measures can be introduced for recycling the energy drawn from the power supply [5] [6].

A novel class of logic circuits called adiabatic logic offers the possibility of further reducing the energy dissipated during the switching events, and the possibility of recycling, or reusing, some of the energy drawn from the power supply. To accomplish this goal, the circuit topology and the operation principles have to be modified, sometimes drastically. The amount of energy recycling achievable using adiabatic techniques is also determined by the fabrication technology, switching speed, and the voltage swing.

III. PRINCIPLE OF ADIABATIC SWITCHING`

The word ADIABATIC comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat [6]. The adiabatic logic is also known as ENERGY RECOVERY CMOS.
With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems.

Adiabatic switching principle is one of the best Power reduction techniques having many advantages over other techniques like simple to design, no complexity increases, and great reduction in power dissipation.

Basically adiabatic switching principle states that during the transition from logic 0 to logic 1 we need the power supply but transition from logic 1 to logic 0. We don't need the power supply. If at that time we make the power supply off we can save the power dissipation because power dissipation is directly proportional to the supply voltage [5][11].

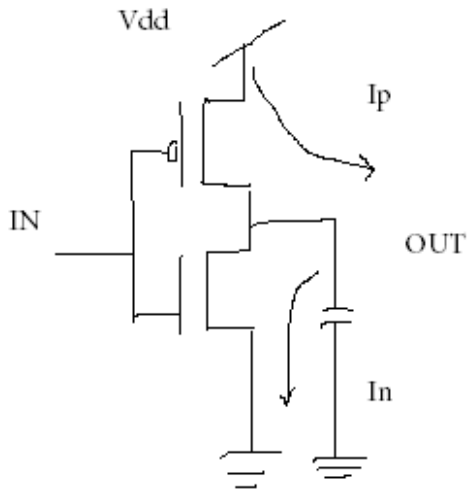


Fig.1 CMOS INVERTER

This can be done by changing the voltage source either by sinusoidal voltage source or by PWL and adjust the supply voltage in such a way that during the transition from logic 1 to logic 0 the supply voltage comes into off state and in this way the power dissipation is reduced up to much extent because as told earlier the power dissipation is directly proportional to supply voltage.

We have to design the supply voltage for every circuit in such a way that maximum power is reduced for every circuit [7] [8].

Further, We will simulate different combinational circuits using adiabatic switching principle and compare the results with conventional circuits[10]& stacking circuits

IV. CMOS COMBINATIONAL CIRCUITS

- Adiabatic technique

A. Design of half adder using adiabatic technique.

Half adder is the basic building block of all Arithmetic circuits. Half adders are present on every microchip or any machine to perform addition, subtraction, division and multiplication. To any half adder we give two binary inputs, namely A and B and two outputs namely sum and carry. The relations between the inputs and the outputs are expressed as:

S=(AXOR B) …(4)
C=A.B …(5)

The adiabatic power supply needs an efficient energy recovery design which implies quality factor Q of the power supply to be very high. Not only the Q should be high, it should be proportional to the cycle time so that the energy dissipation in the power supply should also decrease with the frequency. Otherwise, dissipation in the power supply itself will dominate the logic circuit dissipation at lower frequencies. Most preferable technique is to use sinusoidal voltage supply because of its ease to design as compared to the pure trapezoidal wave [I].

1 –bit adiabatic half adder circuit is shown in fig.1

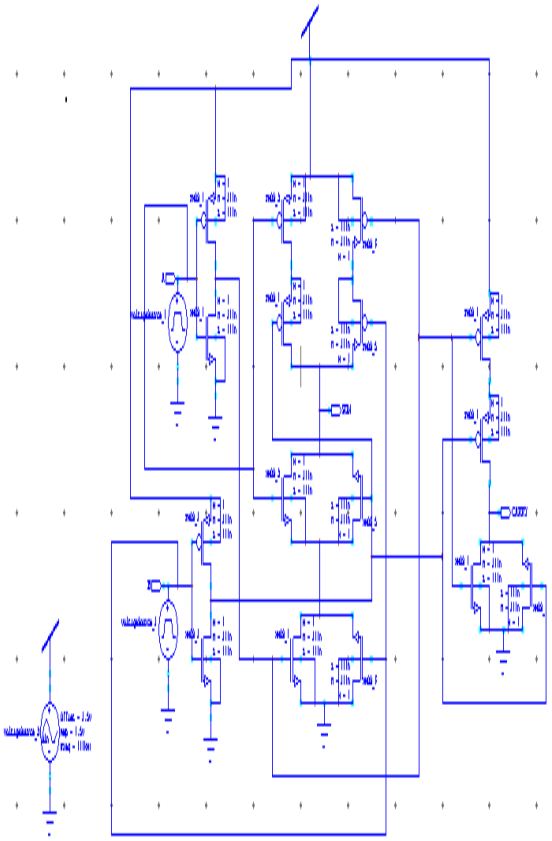


Fig .2 Schematic Diagram of half adder

Using Adiabatic Technique

B. Design of half subtractor using adiabatic technique

The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, A (minuend) and B (subtrahend) and two outputs D (difference) and B (borrow).

The relations between the inputs and the outputs are expressed as:

D=(A XOR B) …(6)

B=(A'.B) …(7)

1–bit adiabatic half -subtractor circuit is shown in fig.2.

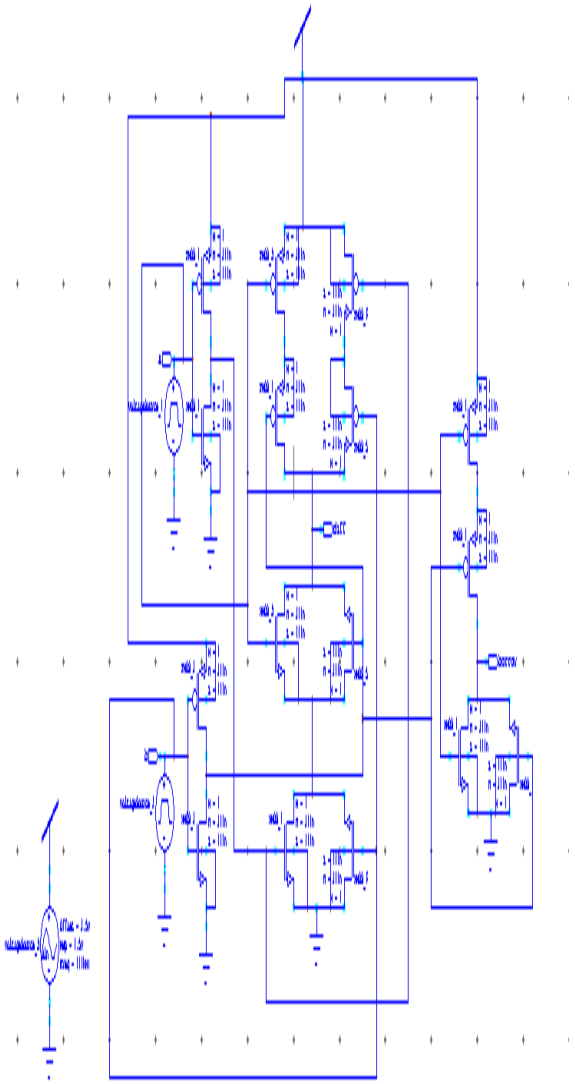


Fig.3 Schematic Diagram of half- subtractor using adiabatic technique

C.Design of 2:1 multiplexer using adiabatic technique

A multiplexer (MUX) is device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has *n* select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector.

An electronic multiplexer can be considered as a multiple-input, single output switch.

In digital circuit design, the selector wires are of digital value. In the case of a 2-to-1 multiplexer, a logic value of 0 would connect I_0 to the output while a logic value of 1 would connect I_1 to the output. In larger multiplexers, the number of selector pins is equal to (Log_2n) where n is the number of inputs.

A 2 to 1 multiplexer has a Boolean equation where A & B are two inputs, C is the select

Input & Z is the output.

Z=(A.C') +(B.C) …(8)

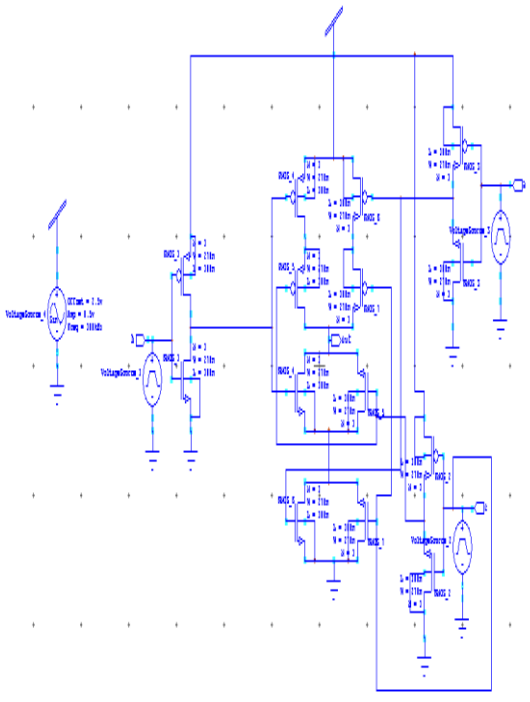


Fig .4 Schematic Diagram of 2:1 MUX

Using Adiabatic Technique

D.Design of 1-bit comparator using adiabatic technique

A digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number.

If we list all the input combinations at The input then we get the following table describing the corresponding outputs.

Equations for f (A>B), f (A=B) and f (A<B) as follow:

(A>B)=(A.B') …(9)

(A<B)=(A'.B) …(10)

(A=B)= (A XNOR B) …(11)

Fig .5 Schematic Diagram of 1 bit comparator

Using Adiabatic Technique

- **Conventional Technique**

A. Design of half adder using conventional technique

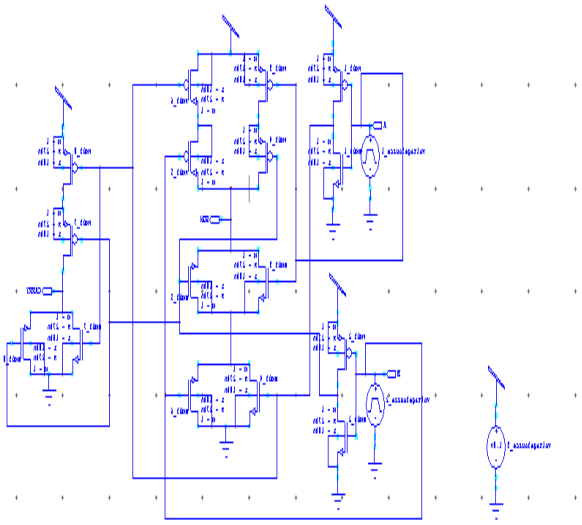


Fig .6 Schematic Diagram of half adder

Using Conventional Technique

B. Design of half-subtractor using conventional technique

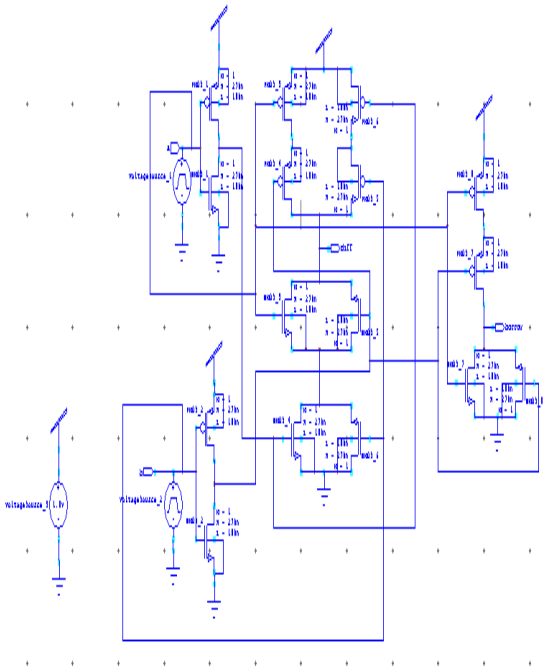


Fig .7 Schematic Diagram of half adder

Using Conventional Technique

C.Design of 2:1 MUX using conventional technique

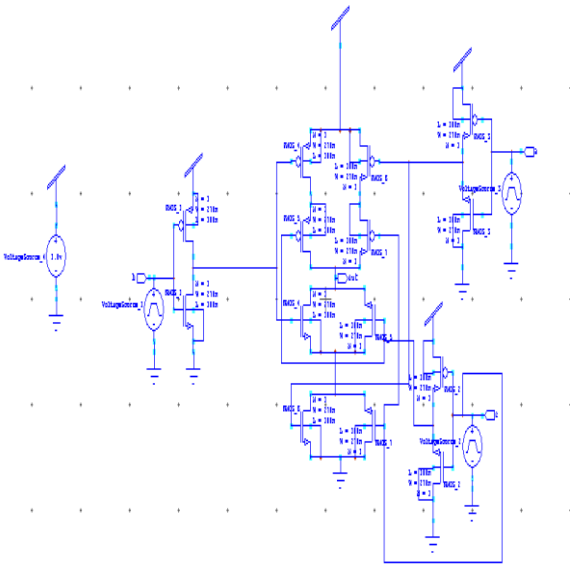


Fig .8 Schematic Diagram of 2:1 MUX
Using Conventional Technique

D. Design of 1-bit comparator using conventional technique

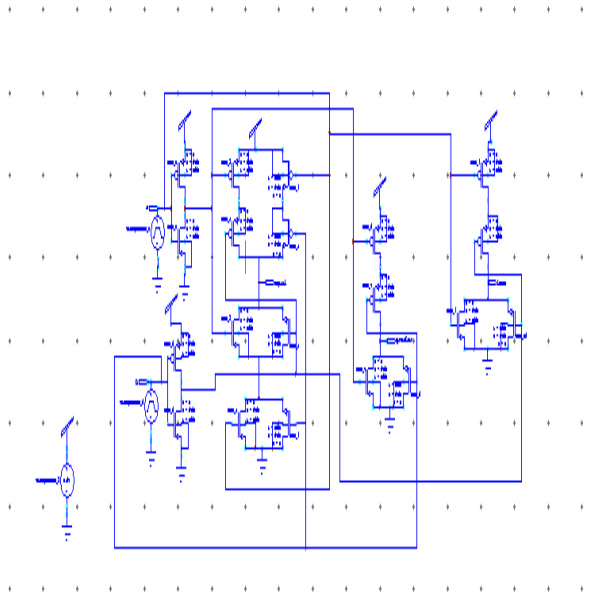
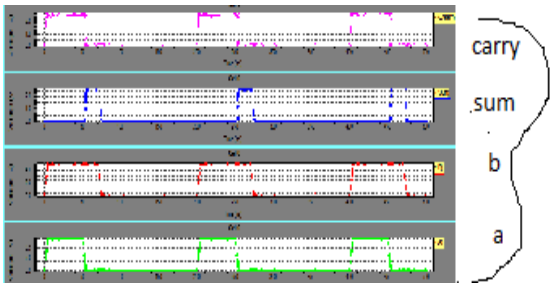


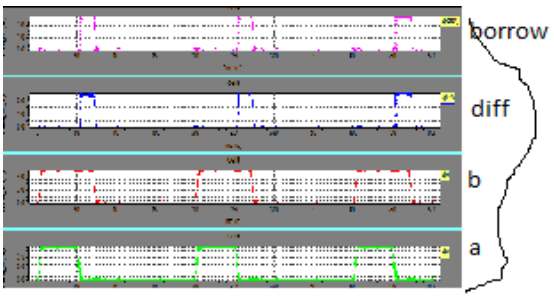
Fig .9 Schematic Diagram of 1-bit comparator
Using Conventional Technique

V. SIMULATION RESULTS

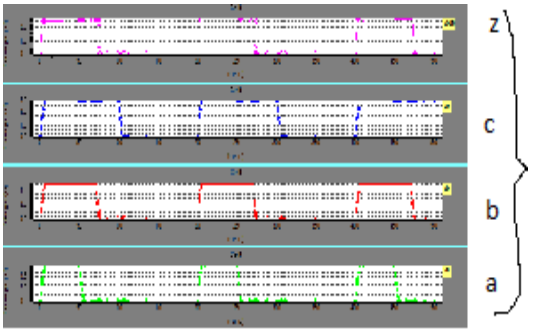
Reduction of power consumption makes a device more reliable. The need for devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies.



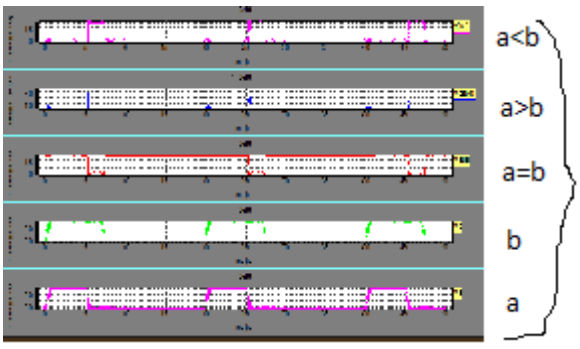
Half adder



Half subtractor

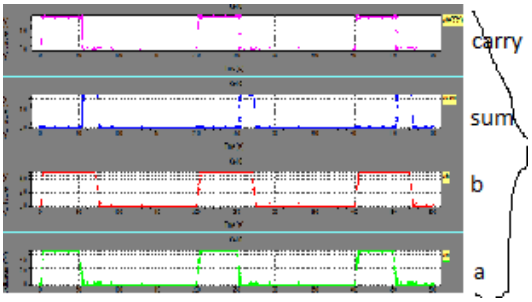


2:1 multiplexer

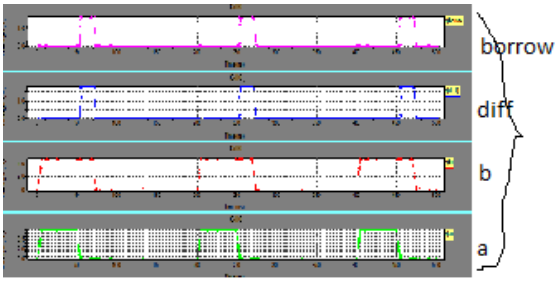


1 – bit comparator

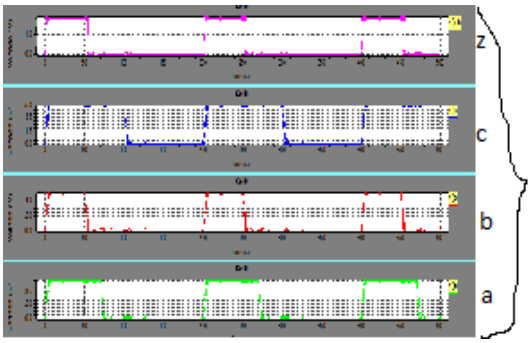
Fig. 10. Simulation results of different combinational circuits using adiabatic technique



Half adder



Half subtractor



2:1 Multiplexer

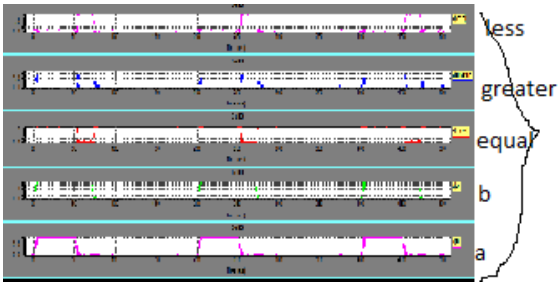


Fig. 11. Simulation results of different combinational circuits using conventional technique

The simulation is done on the 180nm technology [L]. It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component.

As a result, Adiabatic switching principle is Simple to design, no complexity increases, great reduction in power dissipation.

Analysis of this approach shows that by applying sinusoidal ramp, energy saved in the circuit is reduced by the factor of $\Pi^2/8$ compared to pure trapezoidal wave.

Another voltage supply can be designed using PWL in which we ON the supply voltage only when output is logic 1. After simulation, for every combinational circuit power dissipation is estimated.

The 'power dissipation' is a measure of the rate at which energy is dissipated, or lost, from an electrical system.

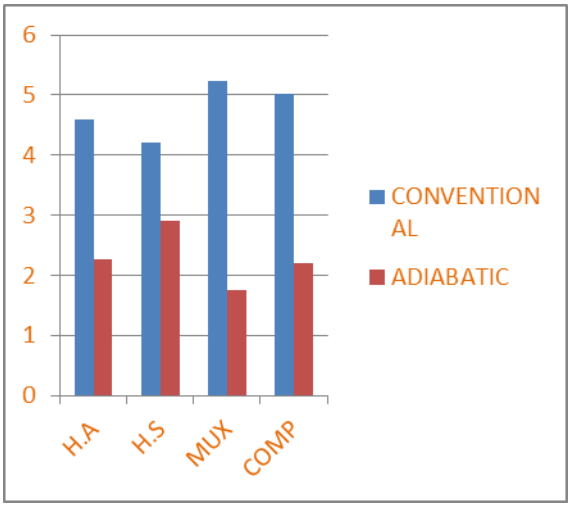
The power dissipation has been evaluated by averaging the power flowing into the combinational circuit.

The comparison of combinational circuits power dissipation with various types of other techniques on which already work is done is in the Table 1.

TABLE 1.

COMBINATIONAL CIRCUITS	ADIABATIC POWER	CONVNTIONAL POWER
HALF ADDER	2.26W	4.62W
HALF SUBTRACTOR	2.91W	4.23W
2:1 MUX	1.75W	5.24W
COMPARATOR	2.22W	5.02W

POWER



CONCLUSION

This paper proposes energy efficient adiabatic logic for digital circuits. The results were simulated using T-SPICE and comparison has been done for power consumption of different combinational circuits for adiabatic logic styles and CMOS design.

The results show that the proposed adiabatic logic has less power dissipation compared to conventional CMOS design and it also uses less power supply. These advantages made this logic more convenient for energy efficient digital applications.

REFERENCES

[1] Rao venkat , Singhal Gaurav Power Issues In Vlsi Design.

[2] Massoud Pedram DESIGN TECHNOLOGIES FOR LOW POWER VLSI

[3] W.C. Athas, etal (1994), "Low power Digital Systems Based on Adiabatic-switching Principles, "IEEE Transactions on Very Large Scale Integration (VLSI) Systems Vol. 2, No. 4, pp. 398-407, 1994.

[4] Hodges, H. G. Jackson, and R. A. Saleh, Analysis and Design of Digital Integrated Circuits, McGraw-Hill, New York, NY, USA, 3rd edition, 2003.

[5] CMOS DIGITAL INTEGRATED CIRCUITS by Sung- Mo Kang and Yusuf Lablebici Tata McGraw-Hill Education, 2003.

[6] Y. Moon and D. K. Jeong, "An efficient charge recovery logic circuit," IEEE Journal of Solid-State Circuits, vol. 31, no. 4, pp. 514–522, 1996.

[7] Ch. Praveen Kumar, S. K. Tripathy and Rajeev Tripathi, "High Performance Sequential Circuits with Adiabatic Complementary Pass-Transistor Logic (ACPL)" IEEE Tencon pp. 1-4, 23-26 Jan. 2009.

[8] Ritu Sharma, Pooja Nagpaland, and Nidhi Sharma, "Analysis of Adiabatic Logic NOR Gate For Power Reduction" International journal of latest research in Science and Technology, vol.1, Issue 2, page No. 179,182,July-August(2012).

[9] N. H. E. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective Addison-Wesley, Reading, Mass, USA, 3rd edition, 2004.

[10] S. Wisetphanichkij and K. Dejhan, "The combinational and sequential adiabatic circuit design and its applications," Circuits, Systems,And Signal processing, vol. 28, no. 4, pp. 523–534, 2009.

[11] A. G. Dickinson and J. S. Denker, "Adiabatic dynamic logic," IEEE Journal of Solid-State Circuits, vol. 30, no. 3, pp. 311–315, 1995.

[12] C. S. A. Gong, M. T. Shiue, C. T. Hong, and K. W. Yao, "Analysis and design of an efficient irreversible energy recovery logic in 0.18 μm CMOS," IEEE Transactions on Circuits and Systems I, vol. 55, no. 9, pp. 2595–2607, 2008.