Logic Gates Using Self-Bias Transistors

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Abstract: **Power dissipation and is the contradicting factors in the design of VLSI CMOS devices. This review paper investigates CMOS circuits with SBT technique with the CMOS. Previous research on circuits shows reduction in power dissipation of combinational circuits by using other different techniques. A Self-bias transistor (SBT) is one which has its gate and drain connected together and works as a current-controlled switch. Here the gate voltage is provided by the drain and MOSFET is always in saturation. As long as a MOS transistor is in saturation region, the current is independent of the drain voltage and it behaves as an ideal current source. Thus power consumption is reduced. Extensive SPICE simulations will be performed with 0.18µm CMOS technology.**

Keywords: CMOS circuits, Power dissipation, Propagation delay, Self-bias transistors (SBTs)

I. INTRODUCTION

One of the key challenges in the integrated circuit industry is designing low-power circuits with high performance. Improving a design relative to power may slow down the circuit, but conversely, an improvement in speed may be achieved only at the expense of power [1].

Consistent with Moore's Law, the feature size of VLSI circuit technology is decreasing at a rate of 0.7 per generation. This rapid change in complexity and density of VLSI circuits gives rise to a number of design issues that were considered unimportant during the predeep-submicron era. The contribution of leakage or standby currents to the overall power consumption of a circuit is one such parameter. The contribution of leakage or standby currents to the overall power consumption of a circuit is one such parameter. While power consumption has been a critical issue in today's VLSI circuits, much of the attention has focused on reducing its dynamic (or switching) component P_{SW}, which is given by

$$P_{SW} = \frac{1}{2} SC_L V_{DD}^2 f \qquad (1)$$

Where S is the switching activity, C_L is the output capacitive load, V_{DD} is the supply voltage, and f is the frequency. Thus, reducing V_{DD} is a popular way of reducing P_{SW} due to its quadratic contribution. However, reducing the ratio of supply voltage to threshold voltage V_{th} increases the delay D of a circuit.

To overcome this effect, threshold voltages are being reduced as well [2]. However, lowering the threshold voltage causes standby currents to increase exponentially due to increased subthreshold conduction. Thus, leakage has become an important component in the power equation and will begin to dominate switching power as feature size continues to decrease [4]–[6]. One efficient method for reducing power dissipation is Self-bias Transistors (SBTs) connected between the pull-up/pull-down network and the supply rails. This technique is presented in [3].

II. CMOS CIRCUIT DESIGN WITH SELF-BIAS TRANSISTORS

A SBT is one which has its gate and drain connected together and works as a current-controlled switch. Figure 1 shows a PMOS and NMOS SBT. Here the gate voltage is provided by the drain and MOSFET is always in saturation. As long as a MOS transistor is in saturation region, the current is independent of the drain voltage and it behaves as an ideal current source seen from the drain terminal. The current through a MOS device in saturation is given by equation

$$I_{dsat} = \frac{1}{2} k_n (V_{GS} - V_{th})^2 \qquad (2)$$

Where, $k_n = k_n' (W/L)$ is the gain factor and $k_n' = \mu_n C_{ox,}$ is the process transconductance of the device. V_{GS} is the gate to source voltage and V_{th} is the threshold voltage of the transistor. Thus by controlling the current through the SBTs we can control the charging and discharging of the load capacitance and hence the dynamic power dissipation which is due to the charging and discharging of the capacitor.

$$C = \frac{1}{V_{DD}} \int Idt \qquad (3)$$

$$P_{dyn} = CV_{DD}f^2 \qquad (4)$$

(a) (b)

Figure 1: (a) NMOS SBT (b) PMOS SBT

Figure 2 shows a CMOS inverter with SBT connected. M1 and M4 are the PMOS and NMOS SBTS respectively. During the active mode, either the NMOS (or PMOS) SBT power gates the pull-down (or pull-up) logic and reduces the leakage current. By adding the SBTs in the

conventional CMOS circuit the effective on resistance got increased. The effective on resistance is given by the equation

$$R_{ON} = \frac{1}{\lambda I_D} \qquad (5)$$

Thus with increase in R_{ON}, I_D will decrease and hence there is a decrease in leakage current. Table 1 shows the power dissipation and propagation delay of with and without SBT connected. It shows that there is a considerable decrease in power. However the propagation delay gets increased.

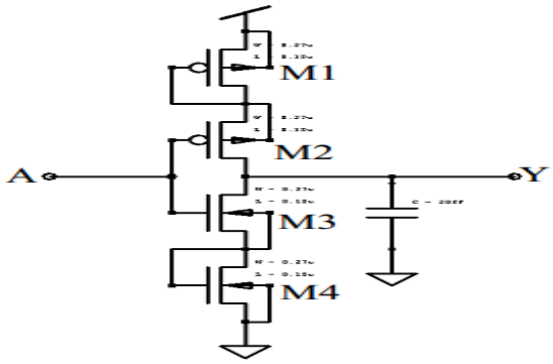

Figure 2: Inverter with SBTs

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