ZCS/ZVS Push Pull DC/DC Converter

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***Abstract*—This paper presents a ZCS/ZVS Push Pull DC /DC converter. The purposed converter that converts a value of direct current to another value of direct current that can produce 250V output voltage from 12V input voltage. Some of the components that use in this paper is a high frequency transformer, and full bridge rectifier. The MATLAB simulation implementation also usesMOSFETs as a switching device due to its high power rating and high switching speed. Consequently, the design circuit will deliver accurate output value with low power losses and small output ripples because this converter has its own filter. The voltage across primary side device is independent of duty cycle with varying input voltage and output power and clamped at rather low reflected output voltage enabling the use of low voltage semiconductor devices. Analysis, design, and simulation results are presented.**

***Index Terms*—ZCS, ZVS, converter, DC/DC, MATLAB, MOSFET.**

I. INTRODUCTION

Transportation electrification has received significant interest owing to limited supply of fossil fuels and concern of global climate change [1-2]. Battery based Electric vehicles (EVs) and Fuel Cell Vehicles (FCVs) are emerging as viable solutions for transportation electrification with lower emission, better vehicle performance and higher fuel economy. Compared with pure battery based EVs, FCVs are quite appealing with the merits of zero-emission, satisfied driving range, short refueling time, high efficiency, and high reliability. A diagram of a typical FCV propulsion system is shown in Fig. 1 [3-5]. A dc - dc converters are widely used in regulated switch - mode dc power supplies and in dc motor drive applications. Often the input to the converters is an unregulated dc voltage, which is obtained by rectifjring the line voltage, and therefore it will fluctuate due to changes in the line voltage magnitude. Switch mode dc - dc converters are used to convert the unregulated dc input into a controlled dc output at a desired voltage level. Converters are very often used with an electrical isolation transformer in the switch - mode dc power supplies and almost always without an isolation transformer in case of dc motor drives.

Bidirectional and unidirectional dc/dc converters are utilized to develop high voltage bus for the inverter. The energy storage system (ESS) is used to overcome the limitations of lacking energy storage capability and fast power transient of FCVs. Bidirectional converter with high boost ratio and high efficiency is required to connect the low-voltage ESS and high voltage dc link bus. Compared with non-isolated topologies, high frequency (HF) transformer isolated converters are preferred with merits of high step up ratio, galvanic isolation and flexibility of system configuration [6]. HF transformer isolated converters could be either voltage-fed [7-9] or current-fed [10-20]. Advantages and disadvantages of both types are compared in [21-23]. The voltage-fed converters have low switch voltage ratings enabling the use of switches with low on-state resistance. This can significantly reduce conduction loss of primary side switches. However, voltage-fed converters suffer from several limitations, i.e. high pulsating current at input, limited soft-switching range, rectifier diode ringing, duty cycle loss (if inductive output filter), high circulating current through devices and magnetics, and relatively low efficiency for high voltage amplification and high input current applications. Compared with voltage-fed converters, current-fed converters exhibit smaller input current ripple, lower diode voltage rating, lower transformer turns-ratio, negligible diode ringing, no duty cycle loss, and easier current control ability. Besides, current-fed converters can precisely control the charging and discharging current of ESS, which helps achieving higher charging/discharging efficiency. Thus current-fed converter is more feasible for the application of ESS in FCVs.

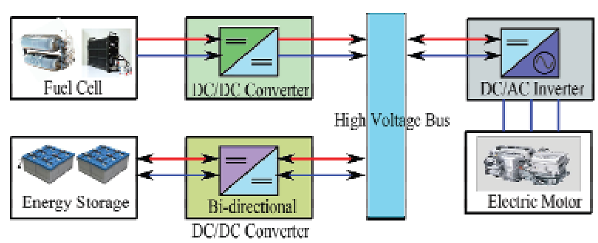


Fig. 1.Diagram of a FCV propulsion system.

The leakage inductance and parasitic capacitance of the HF transformer were utilized to achieve zero current switching (ZCS) in [17-19]. However, resonant current is much higher than input current that increases the current stress of devices and magnetics requiring higher VA rating components. Besides, the variable frequency modulation makes the control implementation difficult and complex [20]. External auxiliary circuits are utilized to achieve ZCS and reduce the circulating current in [26-28] but complex. Although the trapped energy can be recycled, the auxiliary circuits still contribute to a significant amount of loss. In current-fed bidirectional converter, active soft commutation technique [11, 29-30] is proposed to divert the switch current to another switch through transformer to achieve natural or zero current commutation thus reducing or eliminating the need of snubber. In this paper, a push-pull converter is proposed as shown in Fig. 2.

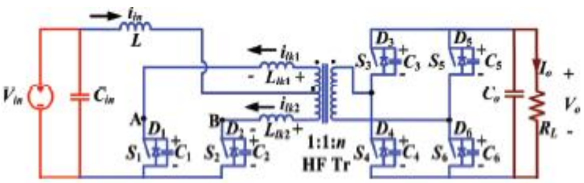


Fig.2. Proposed push-pull DC/DC converter.

A dc - dc converters are widely used in regulated switch - mode dc power supplies and in dc motor drive applications. Often the input to the converters is an unregulated dc voltage, which is obtained by rectifjring the line voltage, and therefore it will fluctuate due to changes in the line voltage magnitude. Switch mode dc - dc converters are used to convert the unregulated dc input into a controlled dc output at a desired voltage level. Converters are very often used with an electrical isolation transformer in the switch - mode dc power supplies and almost always without an isolation transformer in case of dc motor drives.

In thispaper is to design a push pull converter, which can gain output 250V dc from 12V dc input. This work also try to implement MATLAB tools simulation of push pull converter with a center tap high frequency transformer.

The objectives are realized and outlined in various Sections as follows: Steady-state operation of the converter is explained and its mathematical analysis is reported in Section II. Detailed converter design procedure is illustrated in Section III. Analysis and design are verified by simulation results using MATLAB in Section IV. Simulation results of 250V are demonstrated to validate and show the converter performance in Section IV.

II. OPERATION AND ANALYSIS OF THE CONVERTER

For the sake of simplicity, the following assumptions are made to study the operation and explain the analysis of the converter:

a) Boost inductor L is large enough to maintain constant current through it.

b) All the components are ideal.

c) Series inductors L_{lk1} and L_{lk2} include the leakage inductances of the transformer. The total value of L_{lk1} and L_{lk2} is represented as L_{lkT}. L_{lk} represents the equivalent series inductor reflected to the high voltage side.

d) Magnetizing inductance of the transformer is infinitely large.

A. *Boost mode (Discharging Mode) Operation*

In this part, steady-state operation and analysis with zero current commutation (ZCC) and NVC concept has been explained. Before turning off one of primary side switches (say S_1), the other switch (say S_2) is turned-on. Reflected output voltage $2V_o/n$ appears across the transformer primary. It diverts the current from one switch to the other one through transformer causing current through just triggered switch to rise and the current through conducting switch to fall to zero naturally resulting in ZCC. Later the body diode across switch start conducting and its gating signal is removed leading to ZCS turn-off of the device. Commutated device capacitance starts charging with NVC.

The steady-state operating waveforms of boost mode are shown in Fig. 3. The primary switches S_1 and S_2 are operated with identical gating signals phase-shifted with each other by 180° with an overlap. The overlap varies with duty cycle, and the duty cycle should be kept above 50%. The steady-state operation of the converter during different intervals in a one half HF cycle is explained using the equivalent circuits shown in Fig. 4. For the rest half cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle.

Interval 1 (Fig. 4a; to < t < t_1):

In this interval, primary side switches S_2 and anti-parallel body diodes D_3 and D_6 of secondary side H-bridge switches are conducting. Power is transferred to the load through HF transformer. The non-conducting secondary devices S_4 and S_5 are blocking output voltage V_o and the non-conducting primary devices S_1 is blocking reflected output voltage $2V_o/n$. The values of current through various components are:

$i_{S1}=0$, $i_{S2}=I_{in}$, $i_{lk1}=0$, $i_{lk2}=I_{in}$, $i_{D3}=i_{D6}=I_{in}/n$.

Voltage across the switch S_1: $V_{S1}=2V_o/n$.

Voltage across the switches S_4 and S_5: $V_{S4}=V_{S5}=V_o$.

Interval 2 (Fig. 4b; t_1< t < t_2):

At t = t_1, primary switch S_1 is turned-on. The corresponding snubber capacitor C_1 discharges in a very short period of time.

Interval 3 (Fig. 4c; t_2< t < t_3):

All two primary switches are conducting. Reflected output voltages appear across inductors L_{lk1} and L_{lk2}, diverting/transferring the current through switch S_2 to S_1. It causes current through previously conducting device S_2 to reduce linearly. It also results in conduction of switch S1 with zero current which helps reducing associated turn-on loss. The currents through various components are given by

$$i_{lk1}=i_{S1}=\frac{2\cdot V_o\cdot(t-t_2)}{n\cdot L_{lk\_T}} \quad (1)$$

$$i_{lk1}=i_{S1}=I_{in}-\frac{2\cdot V_o\cdot(t-t_2)}{n\cdot L_{lk\_T}} \quad (2)$$

$$i_{lk1}=i_{D6}=\frac{I_{in}}{n}-\frac{4\cdot V_o\cdot(t-t_2)}{n^2\cdot L_{lk\_T}} \quad (3)$$

Where $L_{lk\_T}=L_{lk1}+L_{lk2}$. At the end of this interval t=t_3, the anti-parallel body diode D_3 and D_6 are conducting. Therefore S_3 and S_6 can be gated on for ZVS turn-on. At the end of this interval, D_3 and D_6 commutates naturally.

Current through all primary devices reaches $I_{in}/2$. Final values are: $i_{lk1}= i_{lk2}=Iin/2$, $i_{S1}= i_{S2} =I_{in}/2$, $i_{D3} = i_{D6}= 0$.

Interval 4 (Fig. 4d; $t_3< t < t_4$):

In this interval, secondary H-bridge devices S_3 and S_6 are turned-on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3. At the end of this interval, the primary device S_2 commutates naturally with ZCC and the respective current i_{S2} reaches zero obtaining ZCS. The full current, i.e. input current is taken over by other device S_1. Final values are: $i_{lk1}=i_{S1} =I_{in}$, $i_{lk2}=i_{S2} =0$, $i_{S3} = i_{S6}= I_{in}/n$.

Interval 5 (Fig. 4e; $t_4< t < t_5$):

In this interval, the leakage inductance current i_{lk1} increases further with the same slope and anti-parallel body diode D_2 starts conducting causing extended zero voltage to appear across commutated switch S2 to ensure ZCS turn-off. Now, the secondary devices S3 and S6 are turned-off. At the end of this interval, current through switch S1 reaches its peak value. This interval should be very short to limit the peak current though the transformer and switch reducing the current stress and kVA ratings.

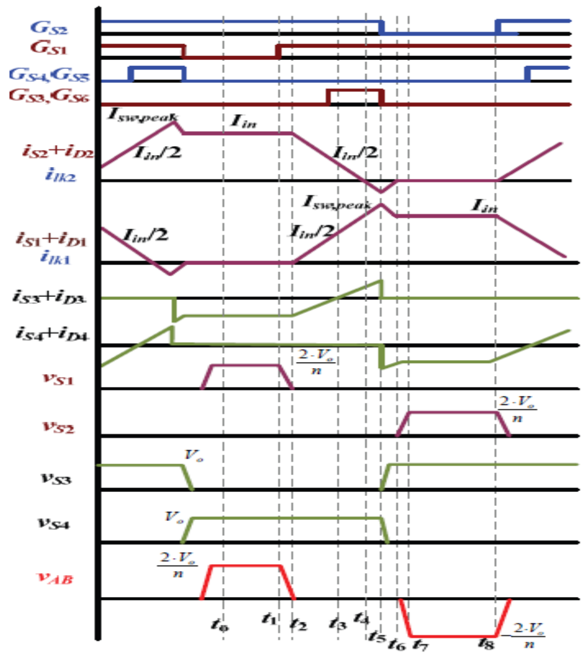
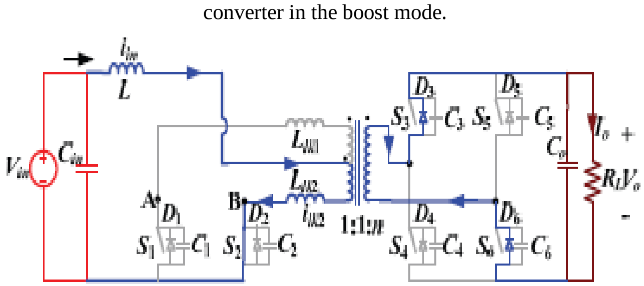
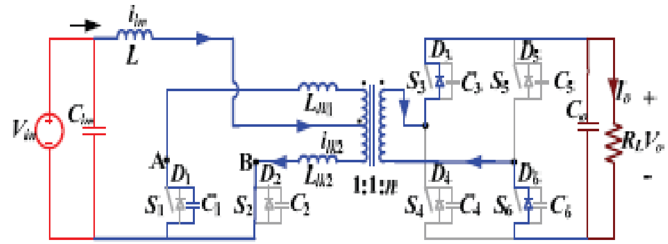


Fig. 3.Operating waveforms of proposed ZCS current-fed push-pull converter in the boost mode.



(a)



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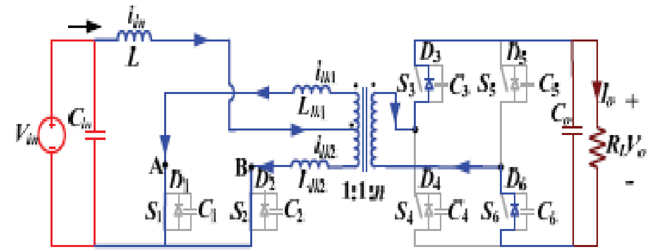

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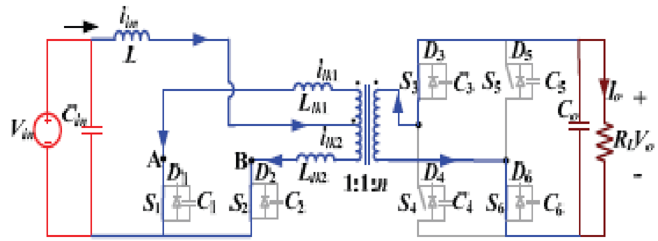

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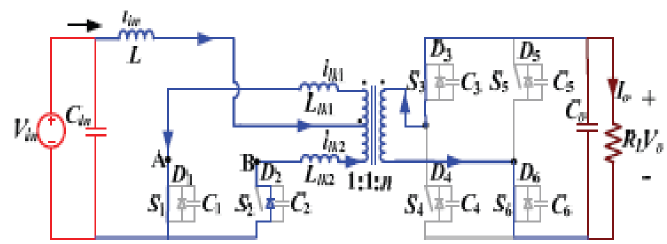

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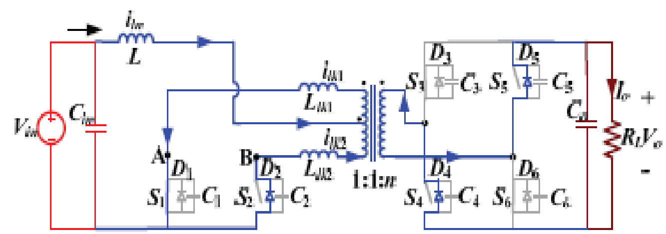

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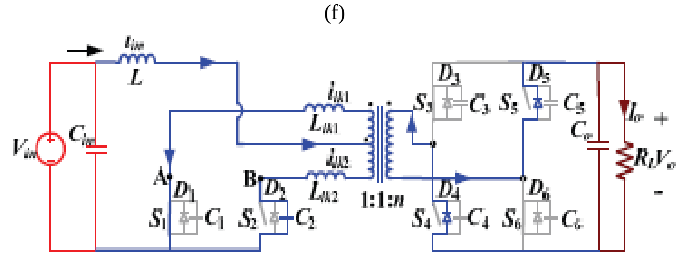
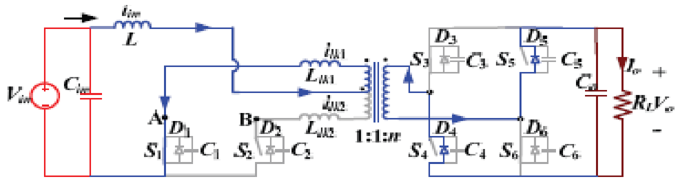


(g)



(h)

Fig. 4.Equivalent circuits during different intervals of the boost mode operation.

The currents through operating components are given by

$$i_{S1} = i_{lk1} = I_{in} + \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_4) \quad (4)$$

$$i_{D2} = -i_{lk2} = \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_4) \quad (5)$$

$$i_{lk1} = i_{S6} = \frac{I_{in}}{n} + \frac{4 \cdot V_o \cdot (t - t_2)}{n^2 \cdot L_{lk\_T}} \quad (6)$$

Interval 6 (Fig. 4f; $t_5 < t < t_6$):

During this interval, secondary switches S_3 and S_6 are turned-off. Anti-parallel body diodes of switches S_4 and S_5 take over the current immediately. Therefore, the voltage across the transformer primary reverses polarity. The current through the switch S_1 and body diodes D_2 also start decreasing.

The currents through operating components are given by

$$i_{S1} = i_{lk1} = I_{sw,peak} - \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_5) \quad (7)$$

$$i_{S1} = -i_{lk1} = I_{D2,peak} - \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_5) \quad (8)$$

$$i_{D4} = i_{D5} = \frac{I_{lk,pea\ h}}{n} - \frac{4 \cdot V_o \cdot (t - t_5)}{n^2 \cdot L_{lk\_T}} \quad (9)$$

At the end of this interval, current through D_2 reduce to zero and is commutated naturally. Current through S_1 reaches Iin. Final values: $i_{lk1} = i_{S1} = I_{in}$, $i_{lk2} = i_{D2} = 0$, $i_{D4} = i_{D5} = I_{in}/n$.

Interval 7 (Fig. 4g; $t_6 < t < t_7$):

In this interval, snubber capacitor C_2 charges to $2V_o/n$ in a short period of time. Switch S_2 is in forward blocking mode now.

Interval 8 (Fig. 4h; t7 < t < t8):

In this interval, currents through S_1 and transformer are constant at input current I_{in} . Current through anti-parallel body diodes of the secondary switches D_4 and D_5 is at I_{in}/n.

The final values are: $i_{lk1} = i_{S1} = I_{in}$, $i_{lk2} = i_{S2} = 0$, $i_{D4} = i_{D5} = I_{in}/n$. Voltage across the switch S_2 $V_{S2} = 2V_o/n$. In this half HF cycle, current has transferred from switch S_2 to S_1, and the transformer current has reversed its polarity.

B. Buck mode (Charging Mode) Operation

In the reverse direction, the converter acts as a standard voltage-fed full-bridge center-tapped converter with inductive output filter. The regenerative braking energy can be fed back and recharge the low voltage storage from high voltage bus, thus increasing overall system efficiency. Standard phase-shift PWM control technique is employed to achieve ZVS of high voltage side and ZCS of low voltage side. At low voltage side, devices need not be controlled because body diodes of the devices can take over as high-frequency rectifier. The steady-state operating waveforms of buck mode are shown in Fig. 5. The secondary side diagonal switch pairs S_3-S_6 and S_4-S_5 operated with identical gating signals phase-shifted with each other by 180o with a well-defined dead time gap. The steady-state operation of the converter during different intervals in a one half HF cycle is explained using the equivalent circuits shown in Fig. 6.

Interval 1 (Fig. 6a; to < t < t_1):

In this interval, secondary side switch pair S_3-S_6 and body diode D_2 of primary side switch are conducting. Power is transferred to the battery from high voltage dc-link bus through HF transformer. The values of current through various components are: $i_{D1} = 0$, $i_{D2} = i_{battery}$, $i_{S3} = i_{S6} = i_{lk} = i_{battery}/n$. Voltage across the diode D_1: $V_{D1} = 2V_o/n$. Voltage across the switches S_4 and S_5: $V_{S4} = V_{S5} = V_o$.

Interval 2 (Fig. 6b; $t_1 < t < t_2$):

At t = t_1, secondary side switch pair S_3-S_6 is turned-off. i_{lk} charge the snubber capacitor C_3 and C_6 and discharges the snubber capacitor C_4 and C_5 in a short period of time. Simultaneously, the capacitor C_1 discharges very fast. At the end of this interval t=t_2, the body diode D_4 and D_5 are conducting. As long as the H-bridge devices S_4 and S_5 are turned on before ilk changes its direction, ZVS turn-on canbe assured. Final values are: $i_{D4} = i_{D5} = i_{lk} = i_{battery}/n$, $i_{D1} = 0$, $i_{D2} = i_{battery}$, $V_{D1} = 0$; $V_{S4} = V_{S5} = 0$, $V_{S3} = V_{S6} = V_o$;

Interval 3 (Fig. 6c; $t_2 < t < t_3$):

Now output voltage appears across inductors L_{lk}, causing current to reduce linearly. The currents through various components are given by

$$i_{lk} = \frac{i_{battary}}{n} - \frac{2 \cdot V_o}{n \cdot L_{lk}} \cdot (t - t_2) \quad (10)$$

$$i_{D1} = \frac{n \cdot V_o}{2 \cdot L_{lk}} \cdot (t - t_2) \quad (11)$$

$$i_{D2} = i_{battary} - \frac{n \cdot V_o}{2 \cdot L_{lk}} \cdot (t - t_5) \quad (12)$$

Final values are: $i_{D4} = i_{D5} = i_{lk} = 0$, $i_{D1} = i_{D2} = i_{battery}/2$.

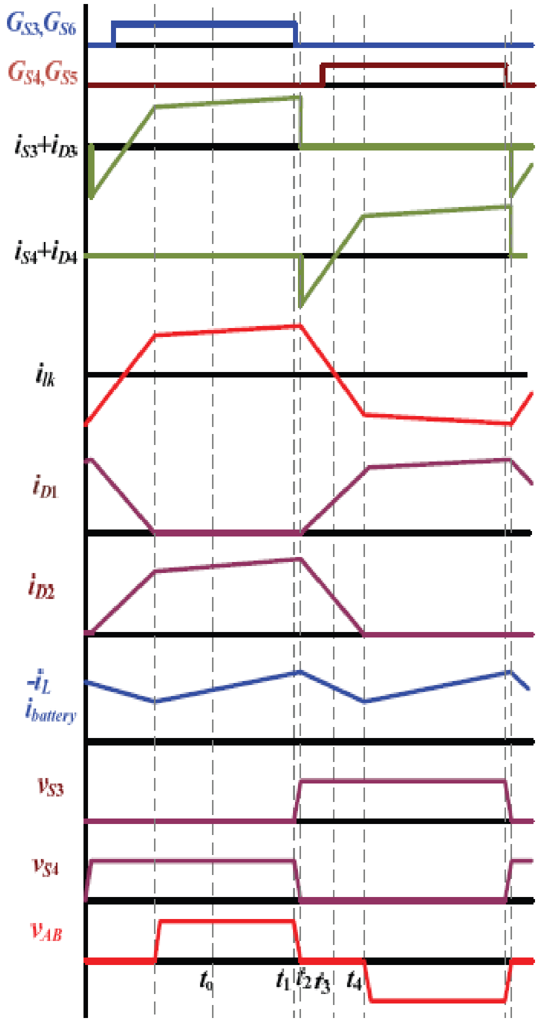


Fig. 5.Operating waveforms of proposed ZCS current-fed push-pull converter in the buck mode.

Interval 4 (Fig. 6d; $t_3 < t < t_4$):

In this interval, S_4 and S_5 are turned-on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3. At the end of this interval, current flowing through body diode D_2 decreases to zero obtaining ZCS. Final values are: i_{lk}=-$i_{battery}$/n, i_{D1} = $i_{battery}$, i_{D2} =0.

III. DESIGN OF THE CONVERTER

In this Section, converter design procedure is illustrated by a design example for the following specifications: input voltage V_{in} = 12 V, output voltage V_o = 150 to 250V, output power Po=200W and switching frequency f_s = 100 kHz. The design equations are presented to determine the components' ratings. It helps selection of the components as well as to predict the converter performance theoretically.

(1) Maximum voltage across the primary switches is

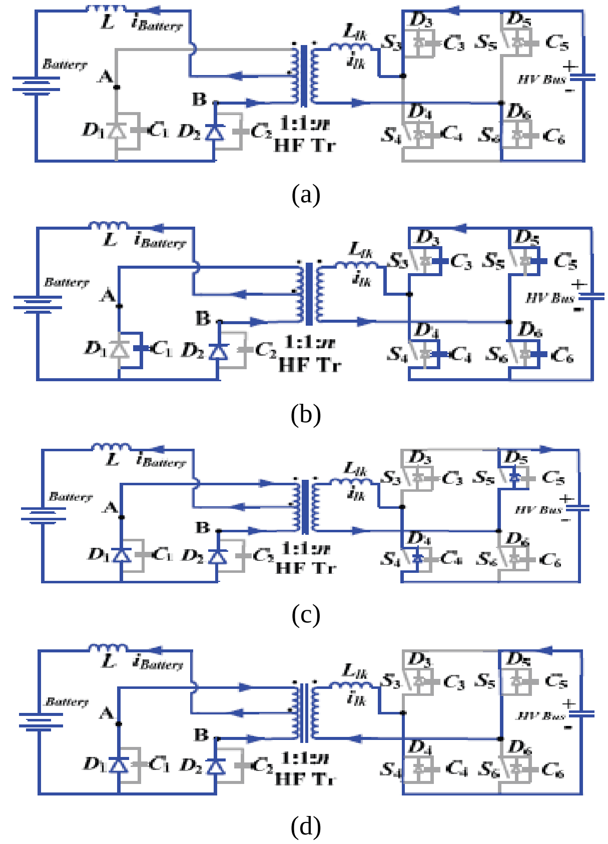


Fig. 6.Equivalent circuits during different intervals of the buck mode operation.

$$V_{p,sw} = \frac{2 \cdot V_o}{n} \quad (13)$$

(2) Voltage conversion ratio or input and output voltages are related as

$$V_o = \frac{n \cdot V_{in}}{2 \cdot (1-d)} \quad (14)$$

where d is the duty cycle of primary switches. This equation is derived on the condition that anti-parallel diode conduction time (e.g. interval 6) is quite short and negligible with the intention to ensure ZCS of primary switches without significantly increasing the peak current. However, at light load condition of converter, (fuel cell stack is supplying most of the power to propulsion system and battery is supplying only auxiliary load), and the anti-parallel diode conduction time is comparatively large, (14) is not valid any more. Due to the existence of longer anti-parallel diode conduction period, the output voltage is boosted to higher value than that of nominal boost converter.

(3) Average input current is $I_{in} = P_o/(\eta V_{in})$. Assuming an ideal efficiency η of 95%, I_{in} = 21.9 A.

(5) The selection of transformer turns-ratio is selected to maintain duty cycle d >0.5. By using (14),

$$n < \frac{2 \cdot V_{o,\min}(1-d_{\min})}{V_{in}} \qquad (15)$$

Therefore, maximum value of n = 12.5 for $V_{o,min}$=150V. Fig. 7(a) shows variation of total value of series inductances L_{lk_T}(H) with respect to power transferring ability P (W) for four values of turns-ratio. With the increase of turns-ratio, the value of L_{lk_T}decreases. It is difficult to realize low leakage inductance with high turns-ratio. In addition, higher turns-ratio may lead to more transformer loss because of higher copper loss, higher eddy current from proximity effect and higher core loss due to larger size. However, increasing the turns-ratio can reduce the maximum voltage across the primary switches, which permits use of low voltage devices with low on-state resistance. Thus conduction losses in the primary side semiconductor devices can be significantly reduced. An optimum turns-ratio n =10, duty ratio d = 0.8 are selected to achieve an acceptable trade-off. Output voltage can be regulated from 150 V to 250 V by modulating the duty ratio from 0.6 to 0.8 including battery voltage variation due to its charging and discharging characteristics.

(6) Leakage inductance L_{lk_T}= 8.18 µH for the given values . Here, series inductors L_{lk1} and L_{lk2} are chosen to be equal to half of L_{lk_T}: L_{lk1}= Llk2=4.09 µH.

Unequal design of series inductors L_{lk1} and L_{lk2} is also permitted.

Push-pull active-clamped current-fed ZVS topology [16-17] and the proposed push-pull current-fed ZCS topology have been The efficiency of the proposed converter is higher due to reduced losses associated with clamp circuit and main primary switches.

IV. SIMULATION RESULTS

Proposed converter has been simulated using software MATLAB. Simulation results for input voltage V_{in} = 12 V, output voltage V_{out} = 250 V, output power P_o = 200W, device switching frequency f_s = 100 kHz are illustrated in Fig. 7. Simulation results coincide closely with theoretically predicted waveforms. It verifies the steady-state operation and analysis of the converter presented in Section II. Waveforms of current through the input inductor L and voltage V_{sec} are shown in Fig. 7. The ripple frequency of input inductor current i_L is 2x $f_s$resulting in a reduction in size. Voltage waveform V_{sec} shows that voltage across the primary switches is naturally clamped at low voltage i.e. $2V_o/n$. Fig. 7 shows current waveforms through primary switches S_1 and S_2 and secondary switches S_3 and S_4 including the currents flowing through their respective body diodes, phase shifted with each other by 180o (S_1vs S_2, S_5vs S_6). Primary switch currents ($I_{(S1)}$, $I_{(S2)}$) are diverted from one switch (say S_1) to the other one (S_2) causing one switch to rise to Iin and the other one to fall to zero. This clearly demonstrates claimed ZCC of primary switches. The negative primary currents correspond to conduction of body diodes before the switches are turned-off, which ensures ZCS turn-off of the primary switches. As shown in current waveforms of S_3 and S_4 in Fig. 7, the anti-parallel diodes of switches conduct prior to the conduction of corresponding switches, which verifies ZVS of the secondary side switches.

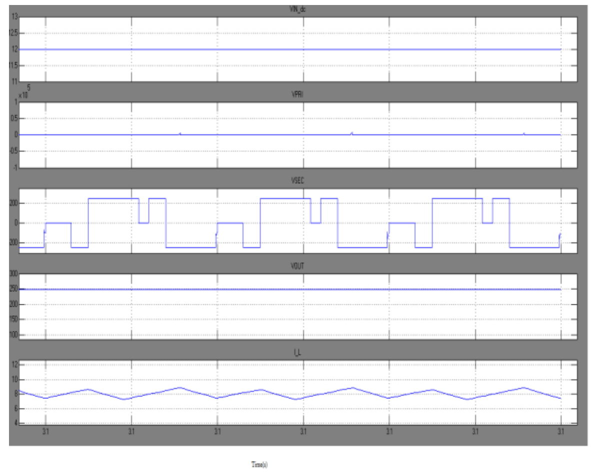


Fig. 7. Simulation results for output power of 200W at out-put voltage 250V. Current through loadi_L and voltage V_{sec}.

V. SUMMARY AND CONCLUSIONS

This paper presents a ZCS/ZVS Push pull DC/DC Converter for application of the ESS in FCVs. A secondary side modulation method is proposed to eliminate the problem of voltage spike across the semiconductor devices at turn-off. ZCS of primary side devices and ZVS of secondary side devices are achieved, which reduces the switching losses significantly. Soft-switching is inherent and is maintained independent of load. Once soft-switching is designed to be obtained at rated power, it is guaranteed to happen at reduced load unlike voltage-fed converters. Turn-on switching transition loss of primary devices is also shown to be negligible. Hence maintaining soft-switching of all devices substantially reduces the switching loss and allows higher switching frequency operation for the converter to achieve a more compact and higher power density system. Proposed secondary modulation achieves natural commutation of primary devices and clamps the voltage across them at low voltage (reflected output voltage) independent of duty cycle. Usage of low voltage devices results in low conduction losses in primary devices, which is significant due to higher currents on primary side. The proposed modulation method is simple and easy to implement. These merits make the converter promising for interfacing low voltage dc bus with high voltage dc bus for higher current applications such as FCVs, front-end dc/dc power conversion for renewable (fuel cells/PV) inverters, UPS, microgrid, V2G, and energy storage. The specifications are taken for FCV but the proposed modulation, design, and the demonstrated results are suitable for any general application of current-fed converter (high step-up). Similar merits and performance will be achieved.

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