Bio-Inspired Ultra Low Power Design of Op-amp with Input Compensation for Biomedical Application (Pacemaker)

Jubin Jain[1], Vijendra Maurya[2] , Anu Mehra[3]

[1]*Department of Electronics & Communication Engineering , Geetanjali Institute of Technical Studies,Udaipur*
[2]*Department of Electronics & Communication Engineering , Geetanjali Institute of Technical Studies,Udaipur*
[3]*Department of Electronics & Communication Engineering , ASET Amity University, Noida*

Abstract: **Due to the rising trends of technologies which are highly inclined towards the low voltage & low power consumption of silicon chip devices which are being developing exponentially due to the rising demand of smaller sized devices which are needed to be operated at lower voltage so that it can support longer battery life which can be used in portable applications such as in marketing segments including telecommunications, biomedical, computers and consumer electronics. It has become major concern that while designing any chip, power consumption is required to be kept in mind especially when it is concerned to biomedical devices. The supply voltage is being scaled down to reduce overall power consumption of the system. The objective of this project is to design ultra low powered operational amplifier which is operated at lower voltage 1.8V. As the voltage is lowered some of the parameters are sacrificed but still it is tried to satisfy the major parameters .It is also not possible to reduce the size of battery upto certain extent due to some chemical limitations, so a pathway is proposed to make the architectural changes. This project showcase the operational amplifier schematic implementation, simulation results with the 0.18µm technology designed in Tanner EDA 14.1. The operational amplifier is used to implement the ADC circuit. The op-amp specially designed for biomedical application (Pacemaker) on an account to improve the battery life of pacemaker.**

The Project will briefly showcase the performance parameter of OPAMP with compensation at input.

Keywords: Power consumption, SNR, Trans-conductance compensation stage, OTA.

I. INTRODUCTION

Several improvements have been done in processing which has pushed the scaling of device dimensions persistently over the past years. The driving force behind this trend is to reduce IC production cost since more components on a chip are possible. In addition to device scaling, the rise in the portable electronics market is also encouraging functioning of device at low voltage and low power circuitry since this would reduce battery size and weight and would enable longer battery life time.

The Operational Amplifier (Op-Amp) is undoubtedly one of the most useful devices in analog electronic circuitry. While designing an op-amp, various electrical characteristics are required to be considered e.g. gain bandwidth, slew rate, common mode range, output swing, offset, power dissipation. Power dissipation of the circuit depends on three parameters frequency, supply voltage and capacitance. If the supply voltage is reduced power consumption can be reduced. But as we keep on decreasing the supply voltage, it also becomes very difficult to drive transistors in saturation region. On an account to achieve the required degree of stability, which is determined by phase margin, other performance parameters are usually compromised. As a result, designing an op-amp must meet all specifications such that it is needed that a good compensation strategy has to be proposed.

A. Operational Amplifier

An operational amplifier (Op-Amp) is a DC coupled input voltage amplifier with high gain. Which is capable of an output voltage a million times greater than the voltage difference across its two input terminals.

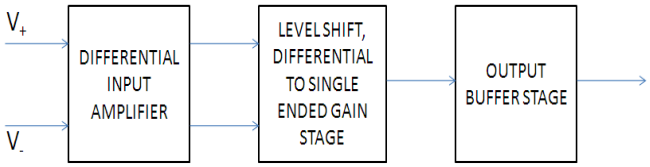

Fig.1. Block Diagram of OPAMP

1. The first block is input differential amplifier, which is responsible for providing very high input impedance, a large CMRR and PSRR, high gain, a low offset voltage, and low noise.
2. The second stage performs Level shifting, added gain and differential to single ended converter.
3. The third block is the output buffer. The output buffer sometimes may be replaced form a high output resistance

un-buffered op-amp often referred to as Operational trans-conductance amplifier or an OTA. Those which have the final output buffer stage have a low output resistance (Voltage operational amplifiers).

B. Old Work

(a). Conventional Design of Two-Stage Op-amp

Basically there are two types of operational amplifiers developed. Operational trans conductance amplifiers such type of amplifier is un buffered op-amp which has high output resistance and the other one is the buffered amplifier which have low output resistance such that is considered as voltage amplifier.
The differential trans conductance stage is introduced in the input of the operational amplifier and sometimes provides the differential to single ended conversion. Normally, a good portion of the overall gain is provided by differential input stage, which improves the noise and offset performance.
The second stage is typically an inverter. If the differential input stage fails to perform the differential to single ended conversion, then it is accomplished in the second stage inverter. The operational amplifier must drive a low resistance load, the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large signal swing.
Bias circuits are provided to establish the operating point for each transistor in its quiescent state. Compensation is required to achieve stable closed loop performance.

(b). Working of Two-Stage Op-amp:

Two-stage OP-AMP mainly consists of a cascade of Voltage to Current and Current to voltage stages. The first stage consists of a differential amplifier converting the differential input voltage to differential currents. These differential currents are applied to a current mirror load recovering the differential voltage. The second stage consists of common source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink load, which converts the current to voltage at the output. The compensation is provided by capacitor to maintain the stability during negative feedback.
The poles moved away from the origin of the complex frequency plane resulting in the negative feedback reducing output resistance.

The conventional op-amp is operated at 3.3V supply voltage. Since major aim of the project is to operate the op-amp at lower voltage 1.8V required for biomedical application.

C. Proposed Design Of Opamp With Input Compensation

The proposed design of opamp is designed to operate at 1.8V with lowered power consumption.

(a). Input Stage:

The key criterion of this project is to operate opamp with lower power supply and to achieve good signal to noise ratio while maintaining less power consumption, low settling time alongwith good reasonable gain. Basically when the bio-potential is sensed its amplitude tends to remain in milli-volts so as to to raise the amplitude of bio-signal, the interfering noise can also be removed which is also important parameter. The task of the input stage of an operational amplifier is of sensing the differential input voltage obtained. This process is disturbed by interference the signals such as offset, bias, drift, noise and common mode noise. The level of these additive inferring signal obtained from other organs of body basically are indicated by the useful sensitivity of the amplifier. The design of the input stage should aim at low values of these interference signals, while the current consumption should tends to remain low, and a large portion of rail to rail range should be available for common mode signals.
The different input topologies are:
1. P-channel and N-channel input stage.
2. CMOS complementary input stage.
When it is needed to keep the SNR ratio as large as possible particularly in case of non-inverting op amp circuits, the common mode input voltage should be kept as wide as possible. This can be achieved by connecting N-type and P-type input pairs in parallel. When two complementary differential pairs are connected in parallel, then it become possible to obtain a rail-to-rail input stage. The NMOS pair tends to remain in conduction state for high input common-mode voltages while the PMOS pair tends to remain in conduction state for low input common mode voltages and both the differential pairs can be operated together for middle values of the input common-mode voltage. But although in such case, the total trans-conductance of the input stage does not remain constant. The constant trans-conductance can also be obtained ; for low-input common-mode voltages only the PMOS pair is active, whereas for high ones only the NMOS pair is in conduction. For middle values, both pairs are "ON," but each with reduced contribution (exactly the half in the "crossing point" condition). The constant-operation with low supply voltages can be obtained by designing input transistors with large aspect ratios tends to operating in weak inversion region.
Since the input transistors are in weak inversion, the input trans-conductance is the same for low and high-input common-mode voltages. For "middle" values of common-mode input voltages, a reduced value of current tends to remain flowing in both the input pairs which is exactly half of the value compared to low and high common inputs. Consequently, the input trans-conductance is always the

same. The input stage mainly comprised of the CMOS complementary stage which is consist of an N-differential pair and a P-differential pair so as to keep the signal-to-noise ratio as large as possible. By introducing current bias transistors the constant current can be maintained in the differential stage. But there is one serious drawback regarded which is the variation of the input stage trans-conductance, g_m with the common-mode input voltage. Such that to cope with it one to three mirrors have been introduced with the such that transistors can be operated in strong inversion region, reducing the variation to about 15%, using a 1.8-V minimum supply voltage.

(b). Output Stage:

Output transistors can be generally being connected in three different ways: Firstly, in a general amplifier (GA) connection (common emitter or common source), secondly, in a voltage follower (VF) connection (common collector or common drain) and thirdly, in a current follower (CF) connection (common base or common gate).

D. Figures & Tables

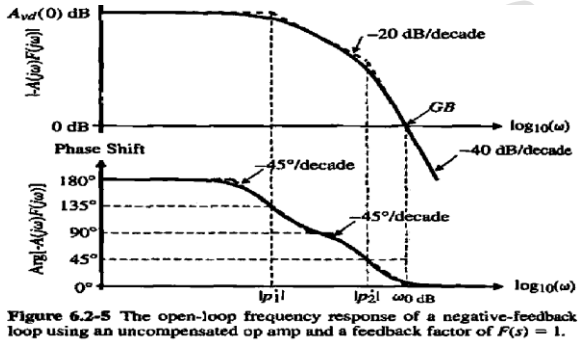

Figure 6.2-5 The open-loop frequency response of a negative-feedback loop using an uncompensated op amp and a feedback factor of $F(s) = 1$.

Fig.2. Ideal Response Of Opamp

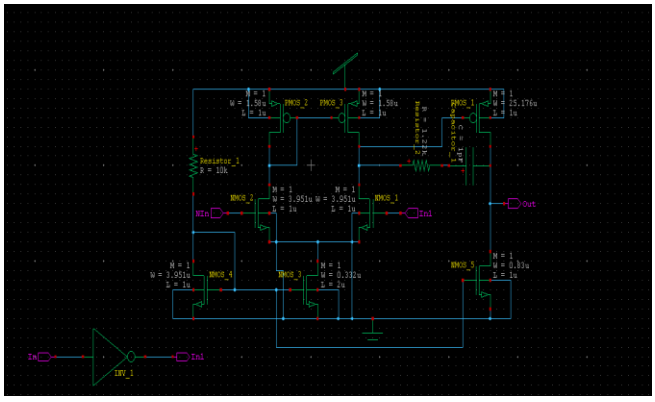

Fig.3.Design of 2-Stage Opamp

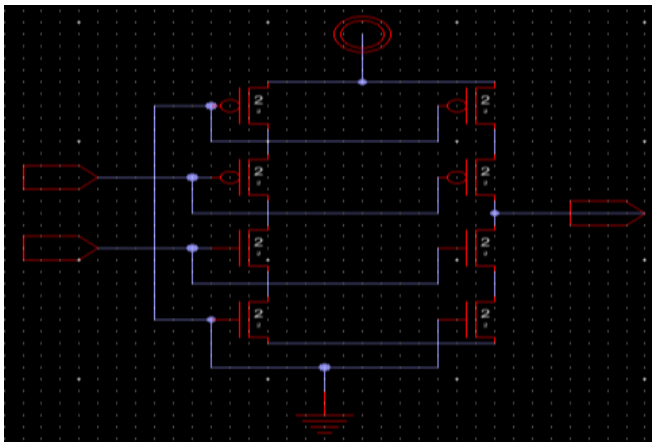

Fig.5. Transconduction Compensation Stage

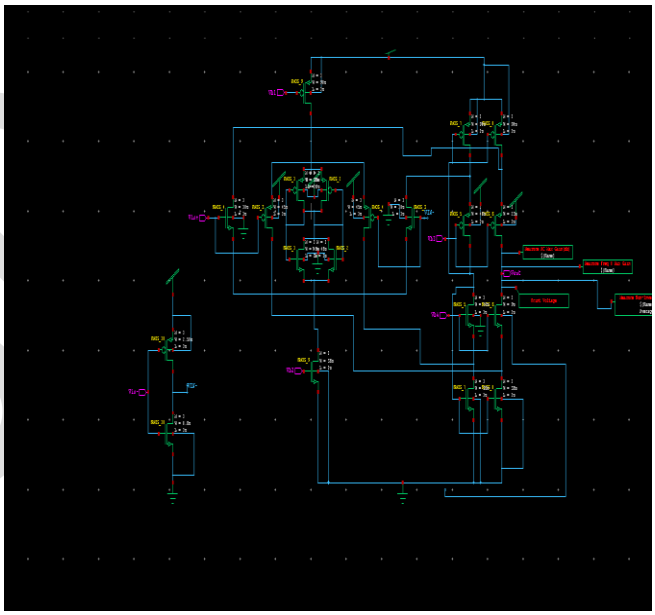

Fig.4.Design of proposed opamp with transconductance compensation

Comparison Table of Two stage opamp & Proposed Design

S.No	Parameters	Conventional Design	Proposed Design
1.	Operating Voltage	3.3V	1.8V
2.	Power Consumption	9.207e-004 W	5.287e-007 W
3.	Unity Gain Frequency	1.0000e+005	1.0000e+008
4.	Phase Margin	55dB	60.25dB

E. Simulation & Results

The schematic is designed using S-Edit tool in tanner EDA 14.1, the frequency response is obtained using W-Edit tool. The 0.18micron technology has been used with 1.8V supply voltage.

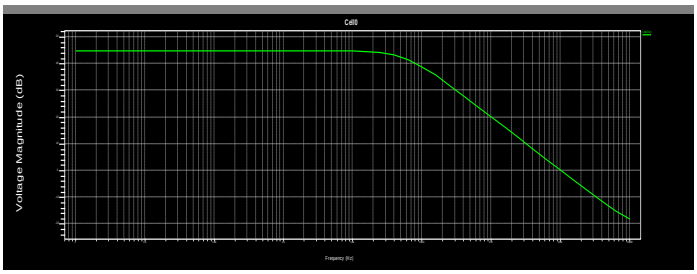

Fig.5. Frequency Response of 2-Stage OPAMP, Voltage Magnitude(dB)

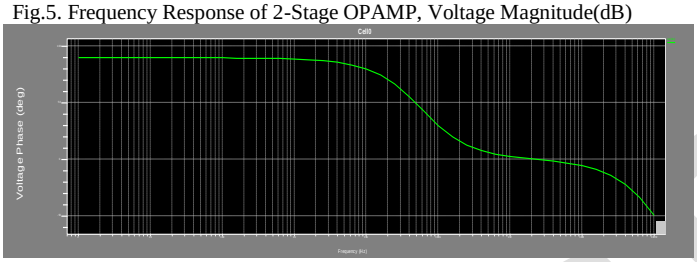

Fig.6. Frequency Response of 2-Stage OPAMP, Voltage Phase(deg)

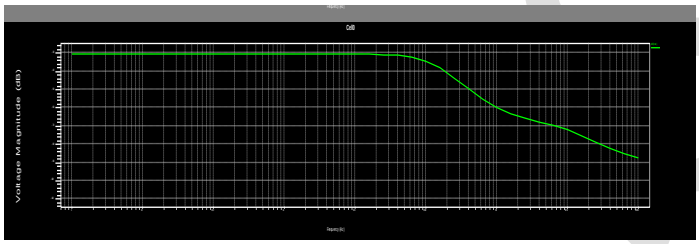

Fig.7. Frequency Response of proposed OPAMP, Voltage Magnitude(dB)

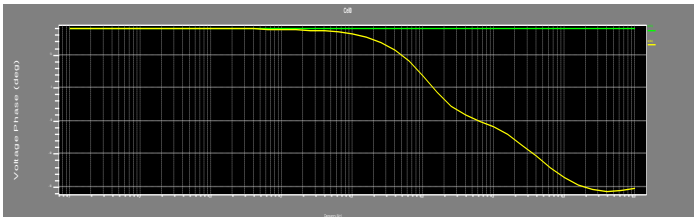

Fig.7. Frequency Response of proposed OPAMP, Voltage Phase(deg)

II. CONCLUSION

In this paper, the input of op-amp stage is compensated due to which result of the output of the OP-AMP doesn't depend on the Trans-conductance. It is achieved by using the complementary differential pair transistors in the push pull configuration. Finally when both the Differential input stage and compensation stage was combined together produce the OP-AMP which is responsible for consuming lesser amount of power with less settling time, Basically the performance of A/D converter is dependent upon settling time. Since settling time means how much amount of time taken by the signal to settle down to its final value, lesser the settling time greater will be the performance of A/D converter and more gain. The proposed design of OPAMP is suitable of biomedical application, Since the main aim of the design is to reduce power consumption for long battery life of pacemaker.

ACKNOWLEDGMENT

We are very thankful to the Geetanjali Institute of Technical Studies supported us a lot to carry out this project successfully.

REFERENCES

[1] A very low power CMOS Mixed-Signal IC for implantable pacemaker applications by Louis S. Y. Wong, Raymond Okamoto.
[2] Design of low power SAR ADC in Biomedical Applications International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Volume 2, Issue 7, July 2013.
[3] Design of Low Power Successive Approximation Analog to Digital Converter Mr. J A. Waghmare et al Int. Journal of Engineering Research and Applications www.ijera.com ISSN : 2248-9622, Vol. 4, Issue 5(Version 7), May 2014, pp.62-66
[4] Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, "Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS," in Proc. IEEE Int. Midwest Symp. Circuits Syst.Dig. Tech. Papers, Aug. 2010.
[5] Euisoo Yoo,Roberts, G.W. "Optimizing CMOS amplifier design directly in SPICE without the need for additional mathematical models", IEEE International Symposium on Circuits and Systems,24-27 May 2009.
[6] CMOS Analog Circuit Design, Philip E Allen & Douglas R Holberg, 2nd Edition,Oxford University Press.