Development of 3-Φ VSI with SPWM Technique Using dsPIC Controller

Dipenkumar H. Kambaliya[1], Niravkumar D. Patel[2]

[1]*Student, M.Tech,* [2]*Asst. Professor, Dept. of Electrical Engineering,*
U.V.Patel College of Engineering, Ganpat University, Kherva
Mehasana, Gujarat, India

Abstract- **Pulse Width Modulation (PWM) is a common technique used in many different applications of 3-phase voltage source inverter. This paper presents a pulse generation of SPWM technique for three-phase voltage source inverter using dsPIC33FJ16GS402 controller. Logic for implementing SPWM technique is described. The carrier signal frequency is designed for 20 kHz with varied modulation index (Ma) and the fundamental signal frequency is designed for 50Hz. Simulation results of controller circuit, carried out in PROTEUS simulator are shown, Also mentioned in developed driver and controller cards in this paper. An experimental result presented in this paper shows the effectiveness of pulse generation Technique.**

Keywords-3-phase Voltage Source Inverter, SPWM, dsPIC, Modulation index (Ma), THD, LC filter.

I. INTRODUCTION

Three -phase voltage source inverters are more common in industrial applications. An inverter is an electrical device that converts direct current (dc) to alternating current (ac); the converted ac can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits.

When any inverter is designed than, the main objective is to minimize the total harmonics distortion of generated output waveform of three-phase voltage source inverter. These converters have many demerits like large size, complicated circuits, more numbers of components are required, more weight, and higher cost.

PWM is a common technique used in many different applications. Up to now, many types of modulating modes have been brought forward in motion control and power conversion, such as classical VSI method, sinusoidal PWM (SPWM), space vector PWM (SVPWM), harmonic elimination PWM and so on [1]. These techniques have some advantages and disadvantages, but the most widely techniques used are the sinusoidal PWM and the space vector PWM.

In a classical VSI (120^0, 180^0 and 150^0) method, the output voltage achieved is equal to a peak supply voltage [3]. Harmonics are also high. The lower order harmonics are present at nearer to fundamental one. In addition, the output rms voltage cannot be controlled(i.e. It remains constant not desired).It is a six-step operation methodology.

To over come this draw back, the modulation pulse methods are implemented[8]. Chopping the voltages and peak harmonics at switching frequency only are the achievements of modulation method. Advantages of this PWM method are as (1) Reducing the total harmonic factor; (2) Lower order harmonic is decreased,(3) Variable rms output voltage(i.e. Output is controllable) is achieving.

Various types of inverters as well as controllers had been designed and implemented which vary from analog and digital circuit controllers, signal processors, micro controller and digital signal processors (DSP). This paper presents a development and implementation of logic for generation of SPWM pulse using dsPIC type controller for three-phase voltage source inverter.

The Block diagram of three-phase inverter is explained in section II. The logic required to develop SPWM pulses are also explained in same section with selection table of dsPIC controller. Section III covers simulation and results of dsPIC using Proteus 7.6 software. All about hardware implementation and its experimental results are covered in last section.

II. IMPLEMENTED SPWM LOGIC USING DSPIC

Block diagram

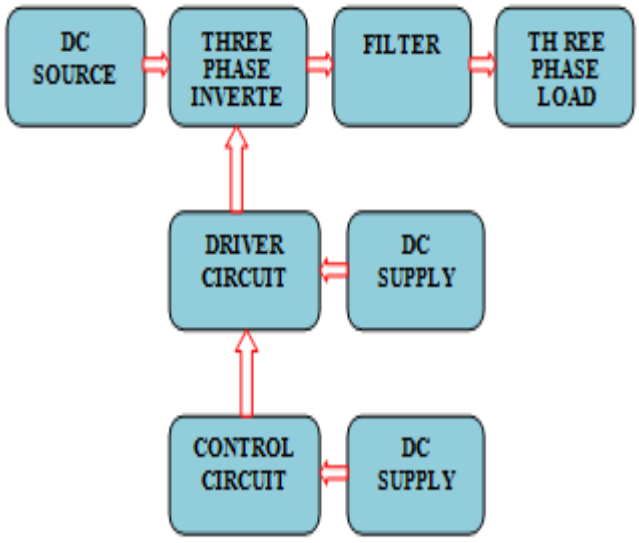

Fig. 2.1: Block Diagram of three-phase Inverter

Block diagram of three-phase Inverter is shown in Fig. 2.1. DC source is used as an input of three-phase voltage source inverter. Three-phase inverter block consist a hex bridge with six IGBT. In control circuit, dsPIC isused for SPWM gate pulse generation. Driver circuit is used for protection against short circuit and protection against dead band. The function of driver circuit is to provide healthy and required pulses for firing of IGBT. The LC filteris used for get smooth sine wave. The ac output of inverter is given to the three-phase load.

Development of Logic for SPWM Pulse Generation

Fig. 2.2 shows the required SPWM pulse pattern for three- phase inverter. The reference waveform is the desired output waveform [4]. Whenever the voltage level of the sinusoidal waveform is higher than the triangular waveform, alogic‘1’signal is generated. Otherwise, it is logic‘0’. As a result, the controller produces SPWM gating signals to turn the switching devices on and off accordingly. Consequently, the inverter produces output voltage waveform resemble to the SPWM waveform. Then, the output voltages pass through the filter to removes higher harmonics from the waveform and make the waveform nearly sinusoidal.

The switching frequency of the SPWM signal is 20 kHz and the frequency of reference signal is 50Hz. So for the SPWM switching technique, total 400 PWM signal is generated. For each quarter cycle of the reference signal, 100 PWM signal is generated. The modulation index Ma can be controlled by varying an ADC cycle [7].

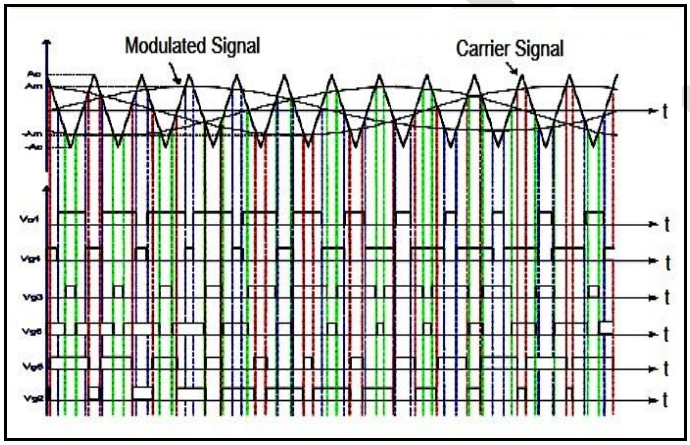

Fig.2.2: SPWM pulse pattern for three phase VSI

If we observe first 100 pulses, which are held between 0to90degreeanglesofreferencewave, the duty cycle is increases. In same manner from 90 to 180 degree, it is decreasing. From 180 to 270, next 100 pulses are in form of decrementing. Once again, they are in incrementing form in 270 to 360 degree. This cycle is repeated at 120 degree apart for second phase and for third phase, it is situated at 240 degree. As we change the modulation index, the pulse width is changed.

Selection of dsPIC for Implementing SPWM Logic

TABLE I: Selection of dsPIC controller

Product Parameter	dsPIC33 FJ16GS 402	dsPIC33 FJ12MC 202	dsPIC33 FJ16MC 304	AT mega 328
No. of Pins	28	28	44	28
Architecture	16	16	16	16
Program Memory	16KB	12KB	16KB	32KB
RAM	2KB	1KB	2KB	2KB
I/O Pins	21	21	35	23
Internal Oscillators	7.37MHz	7.37MHz	7.37MHz	-
CCP	2-std PWM	2-std PWM	2-std PWM	-
MC PWM Ch.	6	6	8	6
Timers	3×16 bit 1×32 bit	3×16 bit 1×32 bit	3×16 bit 1×32 bit	2×8 bit 1×16 bit
SMPS Ch.	6	-	-	-

dsPIC controller consists some futures:(1) three 16 bittimers, (2) 10-bit ADC, (3) PLL logic for increases resolution, (4) immediate update in duty cycle,(5) dead band logic between complimentary pulses. DsPIC33FJ16GS402 is selected based on following table. This controller’s type is16 bitRAM, general SMPS application with 28 pin and 6 SMPS PWM channels [6].

III. SIMULATION RESULTS

The pulse pattern as per discussion is simulated through dsPIC33FJ16MC304 in Proteus 7.6 (simulation software), HTC-Compiler software are used for this simulation as per Fig.3.1.

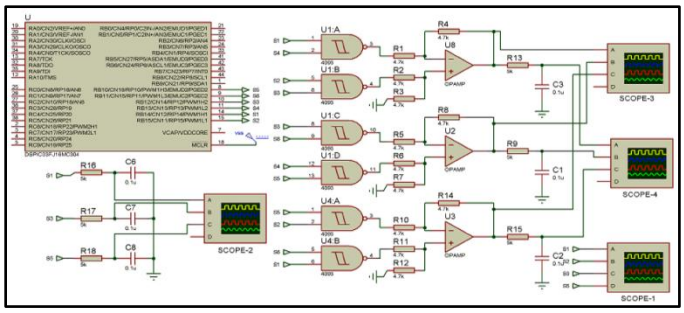

Fig. 3.1: Simulation diagram of SPWM gate pulses generation circuit

Various simulation results areas shown in Figures. Three gate pulses of upper switches of each leg are as shown in Fig. 3.2.Dead band with 2 usec time between to complimentary gate pulse is achieved by dead band register of dsPIC as per Fig. 3.3. Output line voltages across load without RC filter and with RC filter shown in Fig. 3.4 and Fig. 3.5.

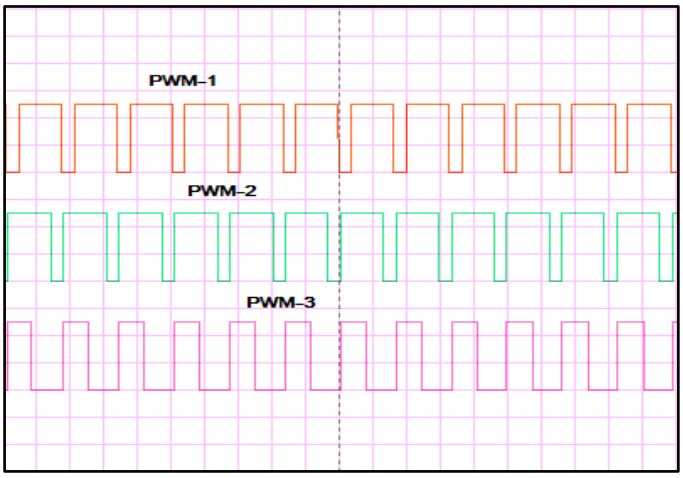

Fig. 3.2: Generated gate pulses for three upper switches. (Scale: x-axis:20usec/div,y-axis:1V/div)

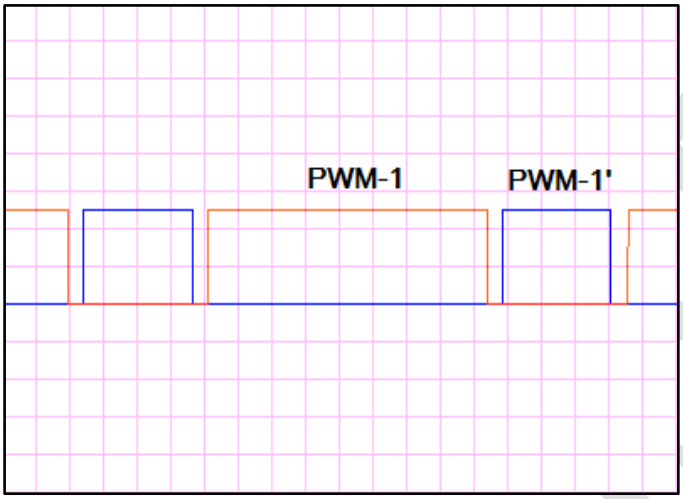

Fig. 3.3: Two complimentary pulses of leg1 with dead band. (Scale: x-axis:5usec/div,y-axis:0.75V/div)

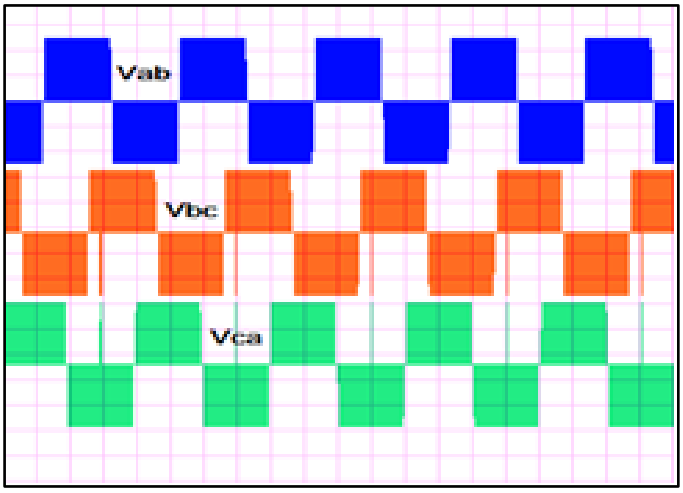

Fig. 3.4: Line to line output voltage waveforms without filter.(Scale:x-axis:5msec/div,y-axis: 2V/div)

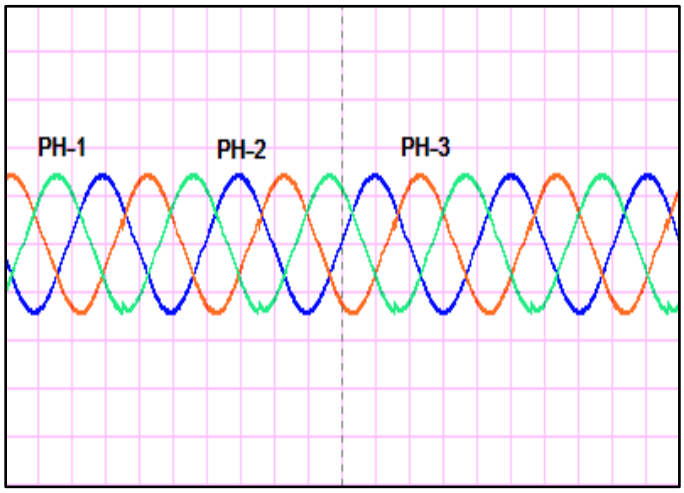

Fig. 3.5: Line to line output voltage waveforms with filter.(Scale:x-axis:2msec/div,y-axis: 1V/div)

IV. HARDWARE IMPLEMENTATION AND RESULTS

Development of Controller Card

Controller circuit block consist a dsPIC33FJ16GS402. It is a 28 pin IC, operated at 3.3 Volt supply. The schematic diagram of developed controller card is shown in Fig. 4.1. Pin 2 is used for changing modulation index based on changing of operated voltage for open loop condition. Output gate pulses are getting from pin21-26.RClogicisalso implemented in this card to achieving three-phase pole voltages.

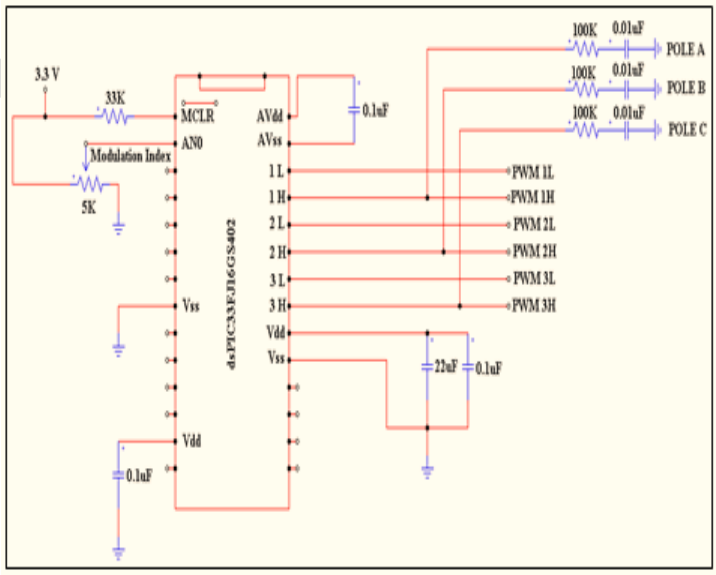

Fig. 4.1: Schematic diagram of developed Controller Card

Fig. 4.2 shows flowchart of dsPIC33FJ16GS402 for SPWM logic, which is implemented for six-gate pulses generation of three-phase voltage source inverter.

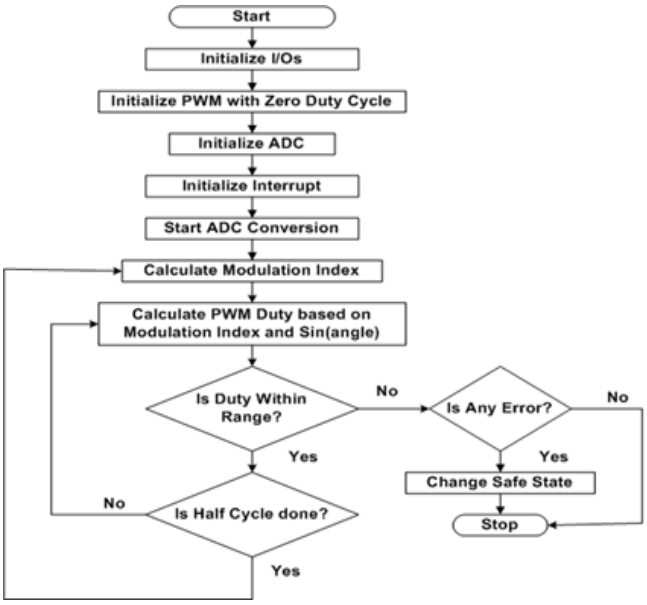

Fig. 4.2: Flow chart for SPWM Technique

The photo view of developed controller card is shown in Fig. 4.3. Regulator unit gives required 3.3 Volts to control unit. Pin 21 to pin 26 of control unit gives required six SPWM pulses. Three upper pulses are connected to RC unit. It is used to check the 120-degree apartness between three legsatany time of testing.

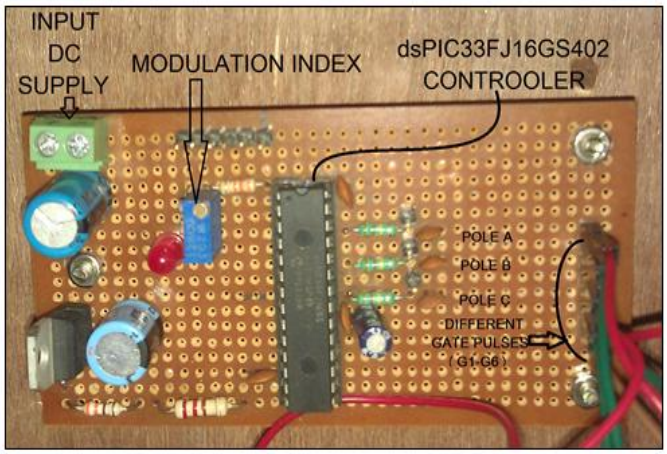

Fig. 4.3: Photo view of developed Controller card.

Various hardware results of SPWM generation circuit using dsPIC33FJ16GS402 are shown here. Generated gate pulses for three upper switches are shown in Fig. 4.4 for 20 kHz frequency. These pulses are 120 degree apart from each. PWM-1and PWM-1' are generated using complement as well as dead band logic which can be implemented using dead band register in dsPIC. Two complimentary pulse ofleg 1 with dead band of 2 micro second are shown in Fig. 4.5. For checking modulation index, RC low pass filter circuit is used in hardware. Output of three pulses with RC low-pass filter with different modulation indexes are shown in Figure 4.6-4.8

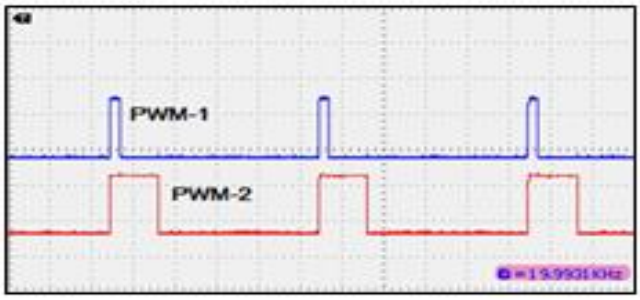

Fig. 4.4: Generated Gate Pulses for upper switches (Scale: X-:10usec/div, Y-:2V/div)

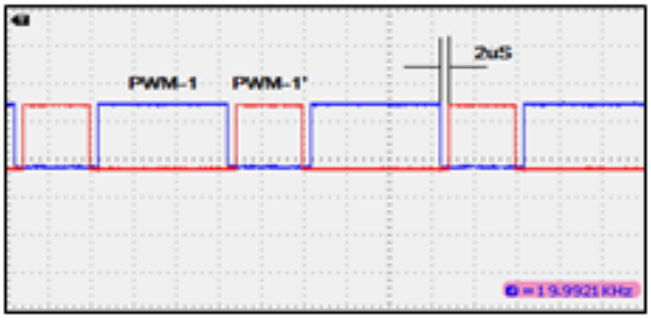

Fig. 4.5: Two Complimentary Pulses with dead band (Scale: X-10usec/div, Y-:2V/div)

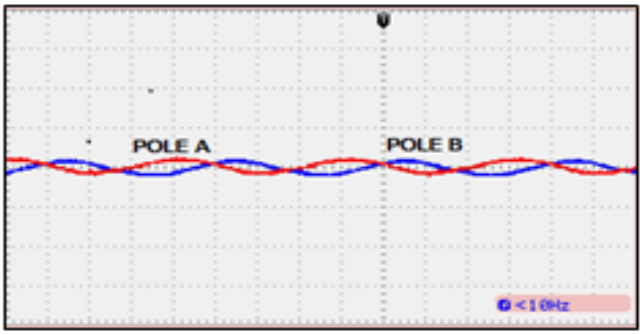

Fig. 4.6: Output Gate Pulse with RC Low pass Filter with Minimum Modulation Index (Scale: X-5msec/div, Y-:5V/div)

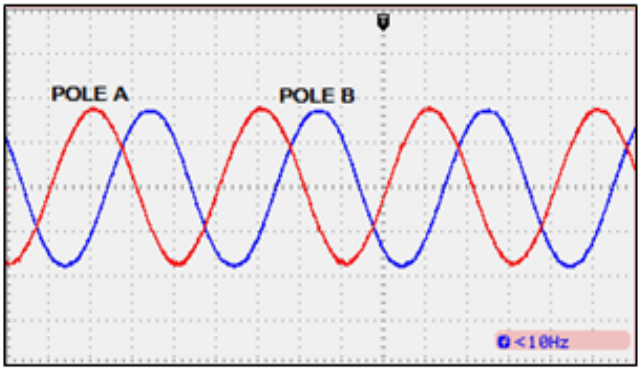

Fig. 4.7: Output Gate Pulse with RC Low Pass Filter with 0.6 Modulation Index (Scale: X-5msec/div, Y-:5V/div)

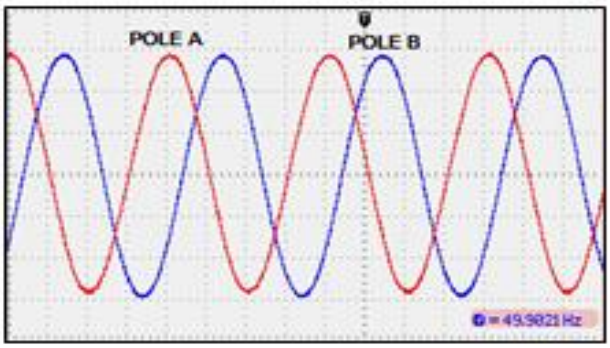

Fig. 4.8: Output Gate Pulse with RC low pass filter with maximum Modulation Index (Scale: X-5msec/div, Y-:5V/div)

Development of Driver Card

Fig. 4.9 shows Driver IC6N137 for SPWM logic, which is implemented for six-gate pulse generation of three-phase inverter. In addition, for protection purpose and healthy pulses required for 3-phase voltage source inverter. It increases magnitude of voltage up to 14.8 V DC if given to 3.8V. Driver card required external DC supply for +5V and +15V.

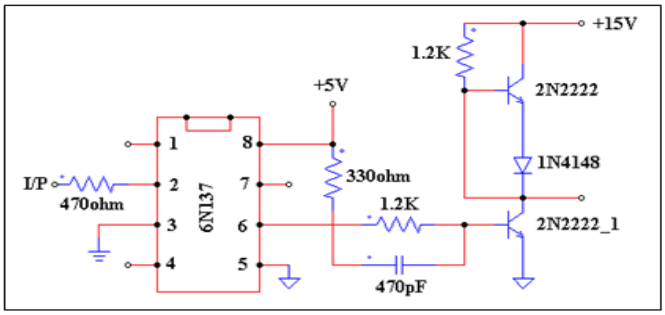

Fig. 4.9: Schematic diagram of developed Driver Card

The photo view of developed Driver card is shown in Fig. 4.10. Regulator unit gives required 3.8 Volts to each Driver unit. Six Driver unit gives required six SPWM pulses. Three upper pulses and three lower pulses. Fig. 4.11 shows Input and Output Signal of Driver IC.

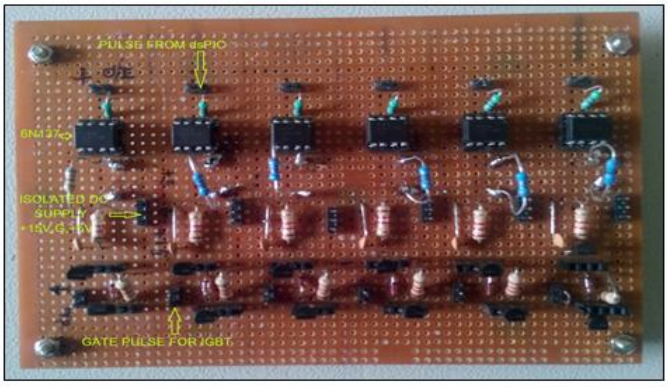

Fig. 4.10: Photo view of developed Driver card.

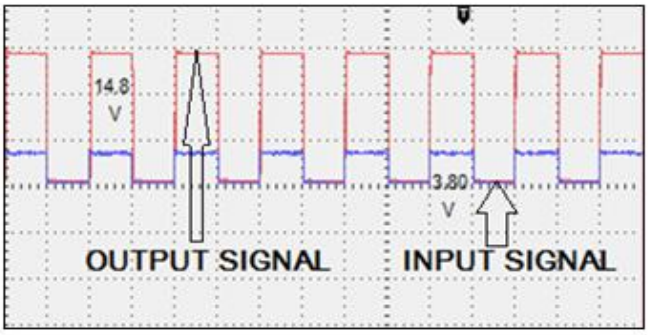

Fig. 4.11: Input and Output Signal of Driver IC (Scale: X-25usec/div, Y-:5V/div)

Fig.4.12 shows the line voltages Vab, Vbc. Each voltage is 120 degree apart from one another. It indicates that pulses are working as SPWM logic. The pulse voltage is 5Volt, so it produces the same level at output side. It indicates accurateness of the logic.

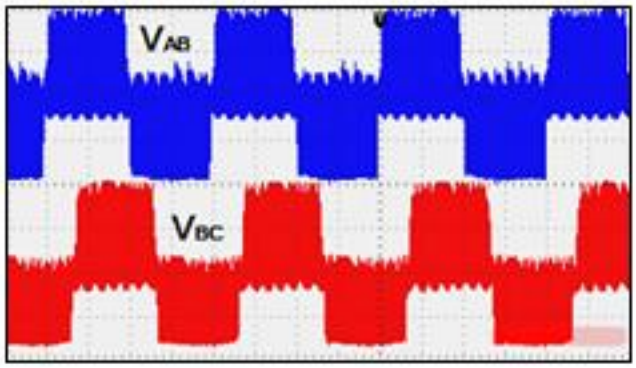

Fig. 4.12: Output Line Voltages with Snubber Capacitor (Scale: X-5msec/div, Y-:10V/div)

V. CONCLUSION

Different topologies are referred for final selection of three-phase inverter. Finally, SPWM topology for three-phase inverter is selected. After topology selection, required components according to given specification for proposed IGBT based three phase inverter is designed. Using the developed logic, simulation is performed in PROTIOUS software. The developed controller has the compact design and it gives an exact SPWM pulses for three-phase inverter using dsPIC33FJ16GS402. Various logics like compliment pulse, dead band, varying modulation index is implemented in dsPIC controller. from hardware results gets 120 degree phase shifted three phase line voltages are achieved using developed control card. Ripple can be reduced using Snubber capacitor across each module. Open loop testing is done till 50 Volt DC (input) with satisfactory results. Controlling is possible from 0.1 to 1 modulation index using developed control card.

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