Multilevel Inverter with Reduced Number of Switches for Solar Energy Generation

Karthikeyan V[1] and Jamuna V[2]

[1]*Assistant Professor, Department of Electrical and Electronics Engineering (Marine), AMET University, Chennai, India.*
[2]*Professor, Department of Electrical and Electronics Engineering, Jerusalem College of Engineering, Chennai, India.*

Abstract **- A New multilevel inverter with reduced number of switches and unequal DC sources is presented. Compared to conventional inverter this inverter produces higher number of output levels with less number of switches and thus harmonics are reduced and the power quality is improved. The switching angles of each level in the output are determined using simple sine property to reduce the output harmonics. The simulation of 33-level asymmetrical multilevel inverter with reduced number of switches is performed using MATLAB/Simulink and the results are presented. The output voltage and current harmonic contents thus reduced are brought to the IEEE standards.**

Keywords **- Multilevel Inverter, BCD topology, Asymmetrical Sources, Total Harmonics Distortion (THD).**

I. INTRODUCTION

The concept of multilevel power conversion dates back to 1980s [1]. Multilevel inverter is the array of power semiconductor switches and DC sources [2]. With proper switching sequence to the switches produces stepped waveform which resembles much to A.C sinusoidal waveform. Hence D.C to A.C conversion is obtained. The advantages of such a method over the conventional method are that the quality of the output waveforms are improved, also it reduces voltage stress on the load and also reduces the switching losses. The application of these inverters includes adjustable speed industrial drives, power quality devices and renewable energy generation [3] such as photovoltaic [4]-[7], wind and fuel cells [1] [2].

Three basic topologies of voltage source multilevel inverter topologies are Diode clamped (DC) multilevel inverter, Flying-capacitors (FC) multilevel inverter, Cascaded H-bridge (CHB) multilevel inverter [1]. In addition, several modulation and control technique have been reported for multilevel inverters [8]. Since the cascaded H-bridge inverter is more popular. Because it reduces the number of hardware components and its reliability is high compared to other multilevel inverter (MLI). The series connection of several H-bridge inverters results the cascaded multilevel inverter. Each H-bridge inverter can produce three levels of outputs ($+V_{dc,}$ 0 and $-V_{dc}$) and their output is represented as V_0 this voltage is sum of output of each H-bridge voltage [7], [9]. This equation is given below,

$$V_o = V_{o1} + V_{o2} + \cdots + V_{on} \quad (1)$$

Fig.1 shows the schematic arrangement of asymmetric cascaded H-bridge inverter.

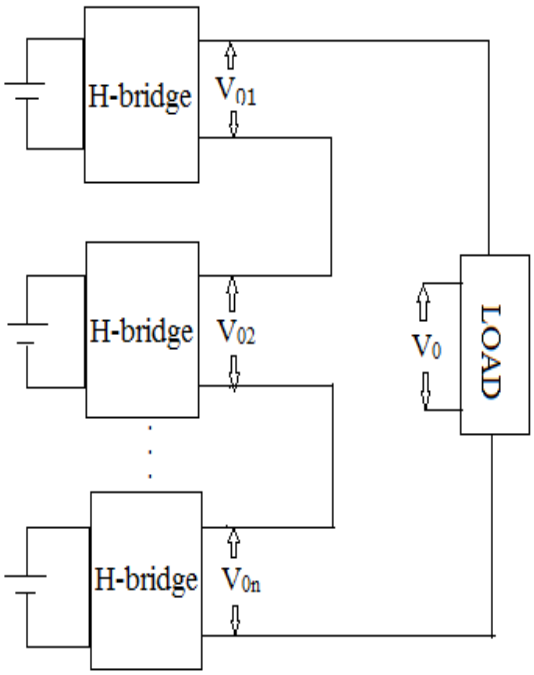

Fig.1 Asymmetrical Cascaded H-bridge multilevel inverter

Cascaded H bridge multilevel inverter is simpler than diode clamped and flying capacitor multilevel inverter topologies because of some advantages such as smaller dv/dt stress, switching redundancy and requirement of least number of Components, no high rated capacitors and diodes [1], [9]. In cascaded multilevel inverter is classified as following types Symmetrical cascaded multilevel inverter and asymmetrical cascaded multilevel inverter [10]. Symmetric cascaded multilevel inverter is one in which the H-bridge units are fed by equal voltages. The effective number of output voltage levels is given by,

$$N = 2m + 1 \quad (2)$$

Where, N denotes the no. of voltage levels and m denotes the no. of. H-bridge units [11].

Asymmetric cascaded multilevel inverters, the H-bridge units are fed by unequal DC sources [11]. The use of multiple DC sources can demand long cables and may lead to voltage unbalance among the sources. This method eliminates the excessively large number of bulky transformers required by conventional multi level inverters [12]. In asymmetric cascaded multilevel inverter DC voltage sources with ratio of binary and ternary [12] are more popular. In binary progression within the H-Bridge inverters, the DC voltages having ratio 1: 2: 4: 8. . , and the maximum voltage levels in the output would be $(2^{N+1}-1)$. While in the ternary progression the amplitude of DC voltages having ratio 1: 3: 9: 27. . , and the output voltage levels will be (3^N) [12]. So, the asymmetrical cascaded inverters are used to provide a large number of output voltage levels without increasing the number of full bridge units.

One main disadvantage of Multilevel Inverter Power Conversion is it requires higher number of switches [13], therefore complexity of the system increases thus the system cost and size. Another is it requires small isolated DC voltage sources or series bank capacitors, in recent years, the research interest on power conversion has been increased substantially to address the above disadvantages [13], [14].

In this paper, a new asymmetrical cascaded multilevel inverter called Binary Coded Decimal (BCD) topology with reduced number of switches is presented. The 33-level inverter simulation model using MATLAB / Simulink is presented. The results of the simulation are also presented.

II. TOPOLOGY DESCRIPTION

In conventional MLI topologies, the number of power switches required depends on the number of levels in the output. This new topology uses less number of switches, while the DC sources are in order of multiples of two or considered to follow the sequence of BCD value $(1 : 2^0 : 2^1 : 2^2 :...: 2^n)$.

Fig.2 shows the circuit diagram of 33-level BCD topology MLI. The circuit can be divided into two parts namely Magnitude Generator and Polarity Generator as used in [15]. The Magnitude Generator can generate all possible positive voltage levels from the different DC sources by proper switching of the switches S_5 to S_{12}. Table.1 gives the switching sequence of magnitude generator part for the different levels of output voltage.

The Polarity generator is a simple H-bridge which simply provides the positive and negative polarity to the output of magnitude generator by reversing the load terminals by proper switching. During positive half cycle, switches S_1 and S_2 are ON, while during negative half cycle, switches S_3 and S_4 are ON.

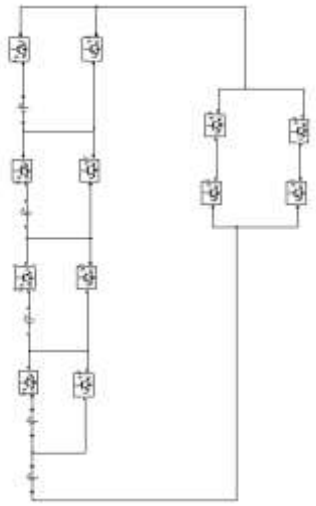

Fig.2 Circuit diagram of 33-level inverter

Table 1 Switching sequence of magnitude generator

Mode	Voltage	SWITCHES							
		S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
1	±15	0	1	0	1	0	1	0	1
2	±30	1	0	0	1	0	1	0	1
3	±45	0	1	1	0	0	1	0	1
4	±60	1	0	1	0	0	1	0	1
5	±75	0	1	0	1	1	0	0	1
6	±90	1	0	0	1	1	0	0	1
7	±105	0	1	1	0	1	0	0	1
8	±120	1	0	1	0	1	0	0	1
9	±135	0	1	0	1	0	1	1	0
10	±150	1	0	0	1	0	1	1	0
11	±165	0	1	1	0	0	1	1	0
12	±180	1	0	1	0	0	1	1	0
13	±195	0	1	0	1	1	0	1	0
14	±210	1	0	0	1	1	0	1	0
15	±225	0	1	1	0	1	0	1	0
16	±240	1	0	1	0	1	0	1	0

III. HARMONIC REDUCTION

The performance of the Multilevel Inverter depends on the proper selection of the switching angles. Switching angles can be found by using any optimization techniques like Newton Rapson method, Resultant theory and Genetic algorithm. These methods require more computational effect. Here the property of the sinusoidal wave is used to find the appropriate switching angles so that the output waveform resembles to sinusoidal waveforms. These angles for 'N' (odd numbered) level inverter can be calculated by,

S_3

$$Sin\alpha(k) = [(k-1) + 0.5]/n \qquad (3)$$

Where, k=1, 2,…....., n & n= (N-1)/2

IV. SIMULATION

Fig.3 shows the simulation model of a 33-level asymmetric cascaded multilevel inverter with reduced number of switches. As shown in MATLAB/Simulink model 12 IGBTs are used. Each IGBT are controlled by individual pulse generator. The load voltage and current are measured.

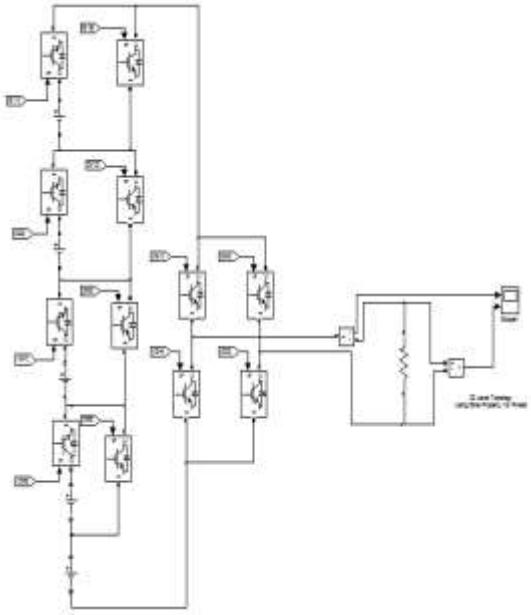

Fig.3 Simulation model of 33-level inverter

V. RESULT AND DISCUSSION

This section shows the simulation results of 33-level inverter for R load and RL load. The simulation is performed in MATLAB and taking 50Hz frequency of operation. The value of R is taken as 50 ohms and the corresponding voltage and current waveforms are shown in Fig. 4 and 6 respectively. The output waveforms are having all the 33-levels as expected. The voltage and current harmonic spectrums are shown in Fig. 5 and 7 and the THD is found to be 2.50%.

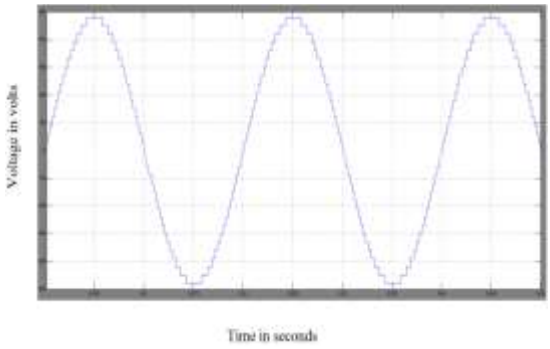

Fig.4 Single Phase output Voltage waveform for R Load

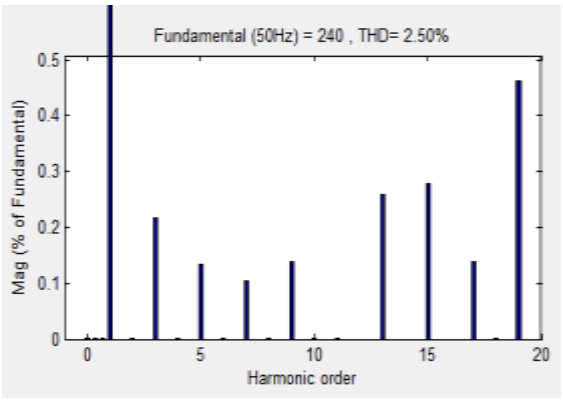

Fig.5 Single phase output Voltage Harmonic Spectrum for R Load

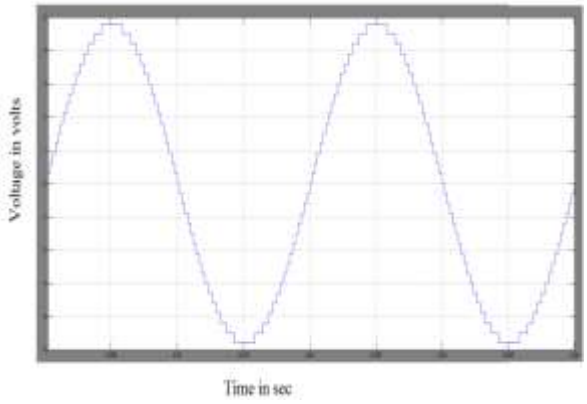

Fig.6 Single Phase output Current waveform for R Load

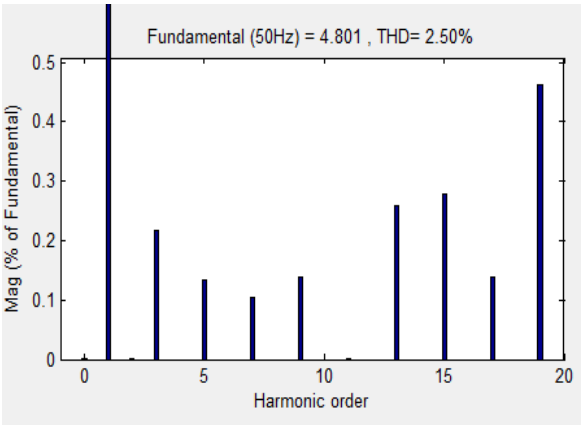

Fig.7 Single phase output Current Harmonic Spectrum for R Load

For simulation with RL load, the value of R and L is taken as 50 ohms and 131mH. The output voltage and current waveforms are shown in Fig. 8 and 10. The output voltage waveform is having 33-levels whereas the current waveform is the smooth sine waveform because of the inductive nature of the load and also there is a phase difference between the voltage and current. The voltage and current harmonic spectrums are shown in Fig.9 and 11. The voltage and current THDs are found to be 2.5% and 0.14% respectively.

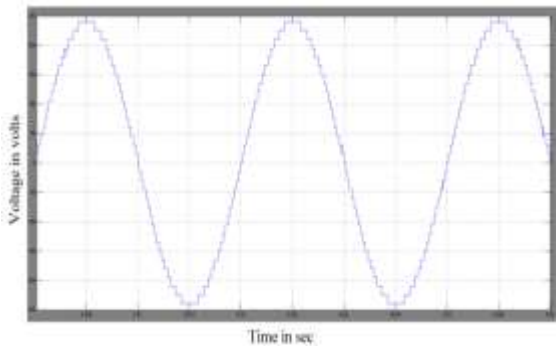

Fig.8 Single Phase output Voltage waveform for RL Load

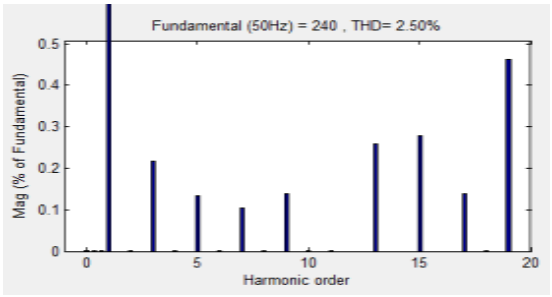

Fig.9 Single phase output Voltage Harmonic Spectrum for RL Load

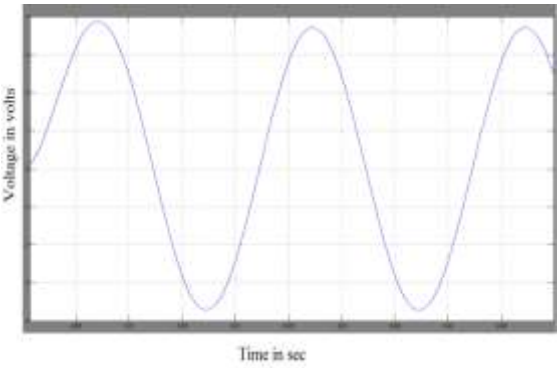

Fig.10 Single Phase output Current waveform for RL Load

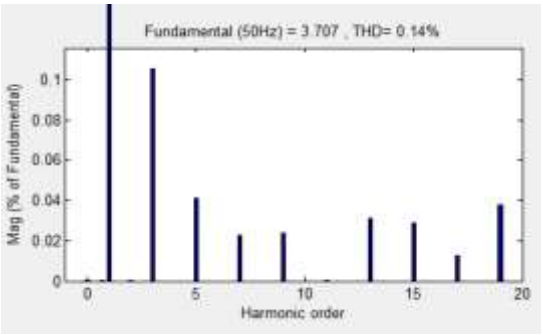

Fig.11 Single phase output Current Harmonic Spectrum for RL Load

VI. CONCLUSION

The operation of new BCD topology with reduced number of switches is discussed and validated with the help of MATLAB/Simulink. The use of simple sine property for finding proper switching angles of each output levels is explained. The output voltage and current waveforms and its harmonic spectrums are presented. These waveforms are similar to the expected. Thus the operation of this topology is validated.

REFERENCES

[1] A. Nabe, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," in Proc. IEEE Industry Applications Society Conference, Sept./Oct. 1980, pp. 761–766.
[2] Jose Rodriguez, Jih-sheng Lai, and Fang ZhengPeng, "Multilevel Inverter: A Survey of Topologies, Controls, and Applications," IEEE Trans. Ind. Applica., vol. 49, no. 4, AUG 2002.
[3] Salvador Alepuz, JosepBordonau, Javier gago, "InterfacingRenewable Energy Sources to the Utility Grid Using a Three-Level Inverter," IEEE Trans. Ind. Applicat., vol. 53, no. 5,OCT 2006.
[4] Carlo Cecati, FabrizioCiancetta, "A Multilevel Inverter for Photovoltaic Systems with Fuzzy Logic Control," IEEE Trans. Ind. Electron., vol. 57, no.12 DEC 2010.
[5] K.Surya Suresh, M.Vishnu Prasad, "PV Cell Based Five level Inverter Using Multicarrier PWM," Int. Journal of Mod. Engg.Rech. vol. 1, issue.2.
[6] Nasrudin A.Rahim, Jeyraj Selvaraj, "Single-phase Seven-Level Grid-connected Inverter for Photovoltaic System," IEEE Trans. Ind. Electron, vol. 58, no.6, JUNE 2011.
[7] Jun Mei, bailuxiao, LeonM.Tolbert, "Modular Multilevel Inverter with New Modulation Method and Its Application to Photovoltaic Grid Connected Generator,"IEEE Trans. Power Electron., vol. 28, no.11, NOV2013.
[8] Keith A. Corzine, Mike W. Wielebski, Jin Wang, "Control of Cascaded Multilevel Inverters," IEEE Trans. Power Electron.,vol. 19, no.3, MAY 2004.
[9] K.Gopakumar, Marcelo A.Perez, Jose Rodriguez, "Survey on Cascaded Multilevel Inverters," IEEE Trans. Ind. Electron., vol.57, no.7, JULY 2010.
[10] Muhammad H. Rashid, "Power electronics: Circuits, Devices, and Applications," 3rd ed. Pearson Prentice Hall, 2004.
[11] Seyezhai R "Multilevel Inverter for Solar Photovoltaic Systems" National Level Workshop on Solar Photovoltaic Systems, 2012.
[12] Dhaval Patel, Himanshu N. Chaudhari, Hina Chandwani & Anand Damle, "Analysis and simulation of asymmetrical type multilevel inverter using optimization angle control technique," International Journal of Advanced Electrical and Electronics Engineering(IJAEEE), vol.1, issue-3, 2012.
[13] Rakesh Kumar, Karthikeyan V, Jamuna V, "A Multilevel inverter with Reduced Number of Switches," National conference on PSPED-2013.
[14] Maruthu Pandi Perumal, Devarajan Nanjudapan, "Performance Enhancement of Embedded System Based Multilevel Inverter Using Genetic Algorithm," Journal of Electrical Engineering, Vol. 62, No. 4, 2011.
[15] Ehsan Najafi, Abdul Halim Mohamed Yatim, "Design and Implementation of a New Multilevel Inverter Topology," IEEE Trans on Ind. Electronics, Vol.59, No.11, Nov'12, pp.4148-4154.