Development of FPGA based Speed Control of Induction Motor

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Abstract: **Since the invention of the wheel there is revolution of rotating machine and the operation of the process has improved. This invention brought the world closer in terms of distance and time. Everywhere the rotating machines were used in different processes. Every moment there is necessity of control of the rotating machine in which the motors are used. The control of the machine is possible with FPGA as it is fast operating device and responds very fast for the changing load and immediately compensates the speed. Fuzzy approach is growing interest in the field of control of various devices. The increasing number of fuzzy applications as well as non linearity handling features and independence modeling requirements, the FPGA is proper choice for control applications. The speed control can be done in various ways and for this purpose now a days the Personal Computer, microcontroller and PLA are used. In different places the speed controller changes are required which is possible using the control devices and at the same time monitoring of various parameters under investigation is necessary. In such cases, the monitoring the various parameters is very essential. The simulation technique provides the better control as well as implementation. The present work contributes towards the speed control of induction motor using PWM technique. In this technique the inverter will be designed for three phase and run by using PWM which conduct one pair of MOSFET leg for120^0.The design of three phase of inverter and its performance testing is carried out and compared with the standard drive available in the market. The testing of the drive performance, efficiency and its speed at various levels is also carried in the present investigation. The different parameter estimation modules are designed around FPGA and tested.**

Key words **: Induction motor drive, MOSFET Inverter, FPGA, PWM control scheme, speed control**.

I. INTRODUCTION

The control devices like Microcontroller, Microprocessor, PLC, PCs availability provides the better facility of digital implementation control signal in the system. The microcontroller along with the PC is commonly used in controlling the various functions of the system under consideration. The increase in control components and parameters along with control signals, the FPGA provides the better flexibly and architecture [1] and provides the support base to the desired application in reduced instructions. The algorithm implementation is quite simple in FPGA and also cost effective. The choppers are essentially used to control the induction motors. This method is simplest and cost effective. The harmonic contents are quite high [2] along with low efficiency at light loads. In order to improve the efficiency and control the speed of the motor, the PWM based inverter system is used. In this control pulses are generated by FPGA which is simple and easier method as compared to else other control methods. Recently Fuzzy logic system is also gaining importance in the speed control applications [3]. Fuzzy logic always deals with uncertainty and member functions with values from 0 to 1. The motor runs at rated speed when connected to power supply. To vary the rotor speed the implementation of fuzzy logic in real time is used. If the load is quite large then speed decreases as well efficiency also decreases. Therefore the poly phase induction motor is used in many heavy duty applications [4]. However the use of PFGA for control of speed and compensate the efficiency software control is used. In the Present investigation PWM control signals were given as input to soft Intellectual Proprietary (IP) core. This in turn allows the motor run at desired speed. The closed loop control system is used for further control of the drive in automated manner [10]. The various parameter sensing modules are developed using FPGA and tested performance of the designed drive in a closed loop.

II. BLOCK DIAGRAM OF SYSTEM DESIGN

Almost all industries require control the speed. The control techniques are different and the presentation of their theory is also different. The development in advanced semiconductor technology boosted the flexibility of the control. The development growth in the initial period was very less at present this rate is increased as the control is now shifted towards the software based simulation and modeling. The feedback systems are deliberately used to adjust the output and to detect the errors. The feedback allows to take the corrective action and maintains the system at some fixed speed. The accuracy in the feed forward system is maintained by the FPGA. In this situation the FPGA has to generate the PWM pulses whose width can be varied using the software. The inverter gain is controlled by PWM pulses generated by FPGA. The PWM pulses are not quite sufficient to drive the MOSFET so buffer is used in which the amplifier serves the purpose of amplify the signal. The isolation is also necessary to separate the power circuit from control circuit.

The system consists of various blocks such as FPGA, single phase rectifier, voltage inverter, driver, signal conditioning circuits, etc. are shown in Fig. 1.

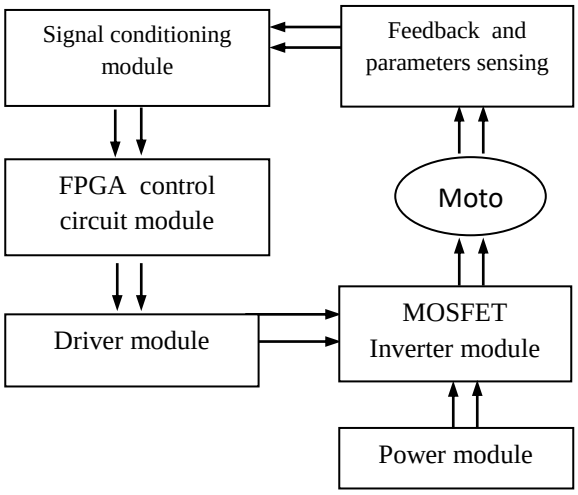

Fig. 1 Block diagram of the FPGA modular drive.

A) Inverter Module

In the present situation the power supplied to the inverter is DC form the power rectifier. This DC power is converted in the AC form by using the inverter circuit. The inverter consists of four MOSFETs which are fired by the PWM signal generated by the FPGA. The firing PWM signal controls the firing of the MOSFET. In this module, PWM firing signal controls the width of the pulse designed through the software. Two signals generated by FPGA are used sequentially for firing of inverter source. While switching of MOSFETs, high currents or transient currents are generated which are bypassed using the snubber circuit consists of capacitor bank, inductor and transistor. The main control unit helps to control the power of the drive and hence the speed of the drive. Depending on the pulse width of the firing pulse, firing of the inverter takes place and proportional power is supplied to the drive. The Fig. 3 shows the implementation of MOSFET based inverter control module. The MOSFET based inverter circuit is shown in Fig. 3

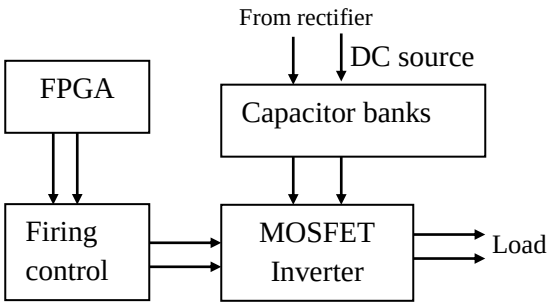

Fig. 2 MOSFET based inverter control

The power supplied to the MOSFET inverter is from the power rectifier. This is a built in rectifier directly used for conversion of 230V AC to DC voltage. The high voltage capacitor series banks are connected across the inverter which helps in rectifying and provides the bypass path to the AC. The transients generated during the switching are easily made ground by these capacitors.

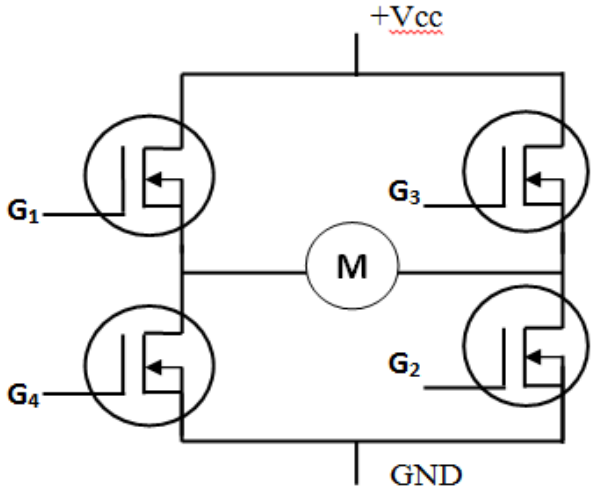

Fig. 3 MOSFET inverter circuit

B) Snubber Module

There are always weak construction features in design of the device and present which leads to damage of the device due to the over heating. In the inverter rapid firing pulses are provided which may generate the surge pulse. To avoid the surge, capacitor and transistor circuit is used. The inductance coil is also connected parallel with this combination. The module is active during the turn off of the firing device. The snubber circuit is used in series with the load to avoid the damage of the load due to reapplication of the input pulses.

C) Driver Module

Generally, the FPGA generated PWM control signal is insufficient to drive the MOSFET, so it is essential to increase the strength of the signal in terms of current. To do so, the buffer circuit is used. The Darlington transistor pair is used in the buffer stage to increase the required current strength. The sufficient gain for firing is achieved by buffer and amplifier complex called as driver. The opto-isolator will isolate the power circuit from the control circuit. This is used for safeguard against any damage if short circuit. The control circuit will be safeguarded using the isolator.

III. POWER CIRCUIT DESIGN

The inverter is designed for 1 HP 800 W single-phase induction motor with power factor 0.9. While designing the power circuit the values of the components are selected in such a way that the power circuit will withstand without any damage and at the same time power dissipation, voltage rating and cost is also taken into account which should be minimum. The inverter is designed for one HP single phase motor. For

which the maximum voltage across the diode bridge is 230 + 10% = 253 V.

The maximum dc output of the bridge is - V_D= 253 x 1.44 = 357 V dc.

Thus the minimum device voltage rating must be 700 V as the diodes are connected in bridge

Selection of MOSFET

The MOSFET is selected on the basis of current rating and type of supply given to the load [5]. The maximum line current drawn by the motor with 0.80 efficiency is –

$$I_{max} = \frac{\text{Wattage}}{V_D \text{ x power factor x efficiency}}$$

$$I_{max} = \frac{800}{357 \text{ x } 0.9 \text{ x } 0.8}$$

$$I_{max} \quad 3.12 \text{ Ampere}$$

$$I_{peak} = 6.24 \text{ Amp. (Peak)}$$

The maximum voltage to the diode bridge is

230 + 10% = 253 Volt.

The maximum output of bridge is -

253 x $\sqrt{2}$ = 357.74 V dc.

Thus taking all factors into account the requirement of minimum device rating must be 357.7 V. With these requirements a switching MOSFET IRF540 is selected, which has built in integrated anti-parallel diode.

Selection Of Diode Bridge

A single-phase diode bridge is designed for low power motor with capacitor filter bank. The maximum input voltage is -

230 + 10% = 253 V.

The maximum output of the bridge is

(253 x $\sqrt{2}$) = 357.7 V DC.

Thus the diode must withstand 357 x 1.5 = 536.5V with derating [6]. The KBP2510 package of bridge fulfils the above voltage condition [7].

Selection of Filter Capacitor

Assuming the voltage drop of 5 % when the input voltage is 230V. The capacitor voltage ΔV = 230 x 0.05 x $\sqrt{2}$

ΔV = 16.261 Volt.

The DC current drawn at full load is I_{dc} which is 6.24 Ampere.

The capacitor value will be a large hence charging time is assumed to be negligible [7-8].

$$I_{dc} = C \Delta V / \Delta t$$

At Δt = 2 m Sec.

$$C = \frac{I_{dc} \text{ x } \Delta t}{\Delta V}$$

$$C = \frac{6.24 \text{ x } 2 \text{ x } 10^{-3}}{16.261}$$

Selected capacitor, C ≅ 767 μF / 500 V.

IV. SIGNAL SENSING AND PARAMETER ESTIMATION

i. Voltage sensing [9]

The peak detector circuit is used for AC voltage sensing shown in Fig. 4. The sensed voltage is in the range of 0-5V, for the variation of 0-230V. After sensing the scaling is essential to get the desired result. The Fig. 5(a) shows the graph of input voltage and sensed voltage. From the figure it is observed that the input voltage and the sensed voltage do not vary in linear way at the initial period, so the correction factor is necessary. The correction factor is applied through the software and the corrected voltage is shown in the Fig.5(b). The graph shows the linear variation of the sensed voltage and corrected voltage.

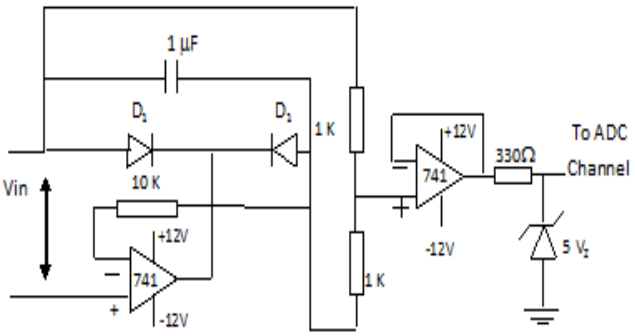

Fig. 4 Peak detector circuit.

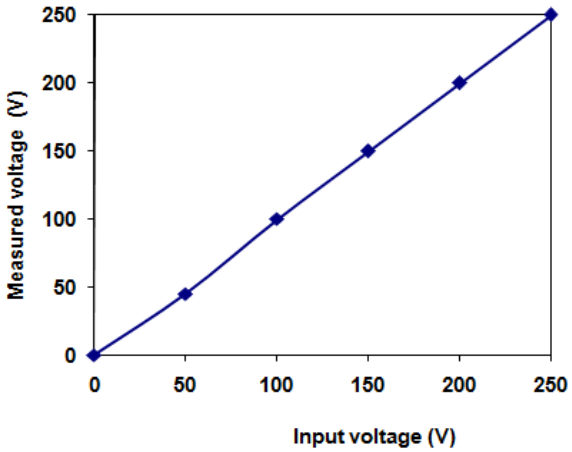

Fig. 5(a) Input voltage versus Measured voltage

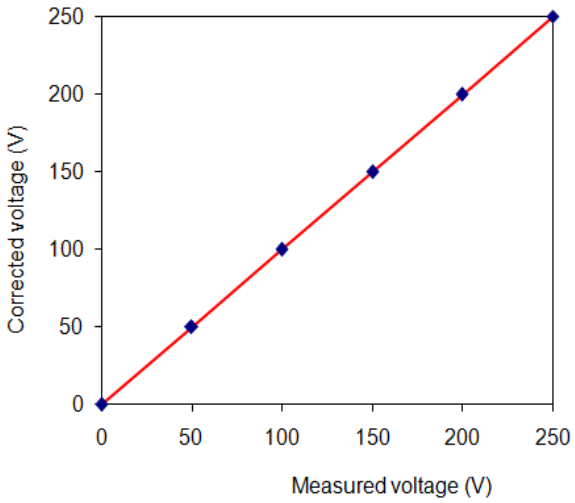

Fig. 5(b) Measured voltage versus Corrected voltage

ii Current Sensing

For measurement of current the simple arrangement is used. Precision value resistance of 1 ohm with 100 W is connected in series with the supply and load. The voltage developed across the precision resistor is proportional to current passing through it. The developed voltage is passed through the transformer and limiter and through the ADC proper voltage is observed. The voltage across the ADC is in the range 0-5V and scaled to 0-15 Ampere. The sensing arrangement is shown in Fig. 6.

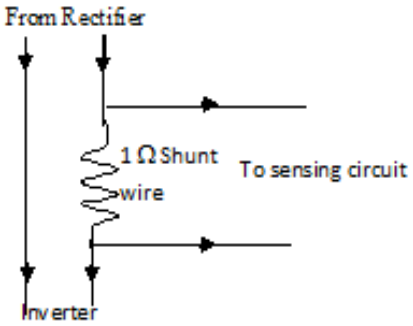

Fig. 6 Current sensing arrangement

iii Speed sensing

For sensing the speed, a circular disk is used which is connected to the shaft of the motor. A hole is drilled across the periphery of the disk. Opto-interruptor device is used having source of light and the detector at other end. The disk rotates between the light source and detector and one pulse per revolution is generated. The number of pulses generated are counted over a specific time interval and the speed is represented in terms of RPM [8]. The Fig.7(a) shows the input speed versus sensed speed.

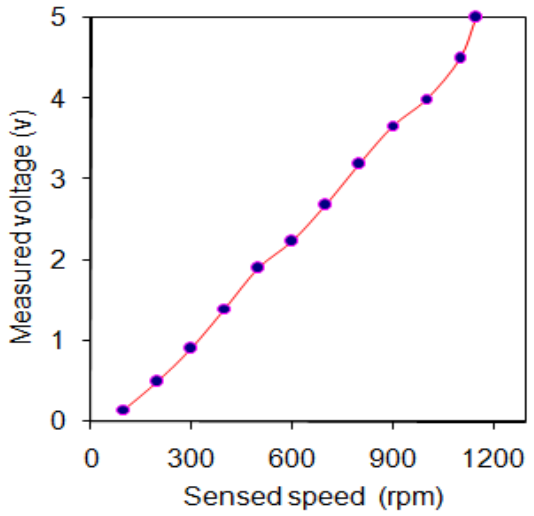

Fig. 7(a) Plot of input sensed speed versus measured voltage

. The input speed shown by tacho-generator and the experimental measured speed shows some non-linear variation at the initial stage. Using the correction factor the variation of the corrected sensed speed is shown in the Fig.7(b).

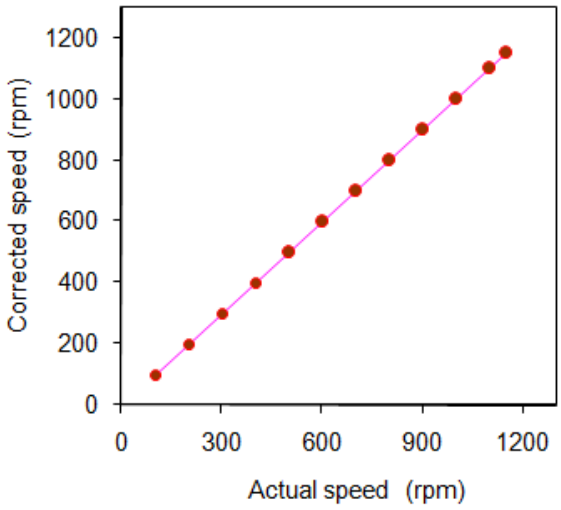

Fig. 7(b) Actual speed of the drive versus corrected speed.

V. RESULTS AND CONCLUSION

The PWM pulses are generated by FPGA and after testing the modular drive for various input voltages and currents. The efficiency is calculated at different speed conditions. The speed efficiency characteristics are shown for single, three five, seven, nine PWM in Fig. 8 for single, three, five, seven and nine pulses per half cycle.

Speed	3PWM	5PWM	7pwm	9PWM
252	49.7	55.8	59.5	54.1

350	54	60.4	63	57.5
500	59	64.4	67.6	62.4
600	62.4	68.1	71.3	66.7
700	66.7	72.1	74.8	70.6
800	71.6	76.3	79	75
850	73.5	78.6	81.8	77
909	76.6	81.2	83.8	79.4
950	78.3	82.5	86	80.7
1000	80.3	84.7	88.8	83.4
1095	83.2	87.7	91.5	86.7
1150	84	87.5	91	87
1250	79.2	77.7	76.1	83.2

Table 1. Speed efficiency data

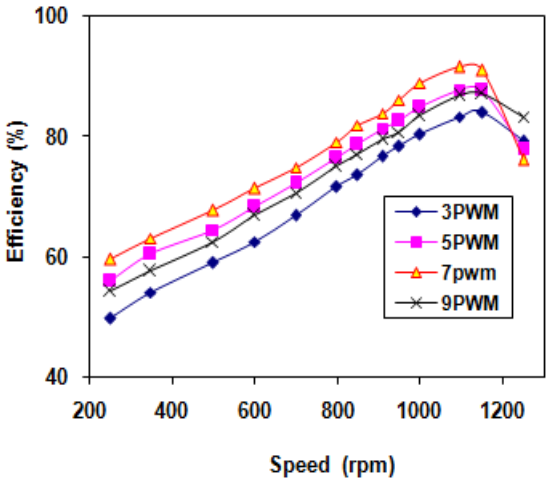

Fig.8 Speed efficiency Characteristics of drive.

It is observed that the variation is linear up to the speed 1095 rpm and then efficiency decreases. It is also seen that the speed increases the efficiency also increases till the 1095 rpm. The efficiency of nine PWM decreases than the seven PWM scheme indicates that the switching losses increases. The best firing scheme is seven pulses per half cycle should be implemented for better results and efficiency of the machine. Fig. 9(a) and 9(b) are the PWM pulses for firing of inverter for five and seven pulses per half cycle.

Fig. 9(a) 5 pulse PWM Generation

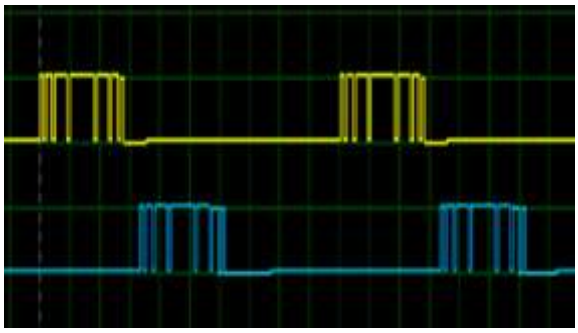

Fig. 9(b) 7 pulse PWM Generation

The PWM technique used for precise speed control of the drive. The firing of the inverter is done by PWM pulses generated by the FPGA. The variation of the pulse width of the generated pulse varies the speed i.e. increase in pulse width will provide more power to the drive as MOSFET will fire for longer time and speed is more. While decrease in pulse width, speed is less. The width of the firing pulse controls the power and hence the speed of the drive. The results indicated are well within the acceptable range. The deviation the results are due to the losses in the machine and switching of the inverter. The developed drive is suitable for the industrial application.

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