Study and Analysis of Switched Mode DC – DC Converter Topologies for Telecommunication System

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***Abstract*: The growing trend in power demand and efficiency requirements of modern telecommunication systems is in need of PFC converter at the front end. The presence of non-linear loads results in poor power factor. Also, there is a need to reduce the ripple present at both the input and output end of the DC to DC boost converter so as to improve the supply power factor of the system. This paper reveals a comparative study of ripple present in inductor current, output current and output voltage of three different topologies of DC-DC converters namely dc-dc boost converter, interleaved boost converter and soft switching interleaved boost converter. This paper also highlights the significance of each converter by computing the efficiency. The simulated waveforms have been demonstrated using MATLAB/SIMULINK. The performance of three different dc – dc boost converter topologies is investigated and the results are verified. The results reveal that soft switched gives a higher efficiency compared to the other topologies.**

***Key words*: Boost Converter; Interleaved Boost Converter (IBC); Soft Switching Interleaved Boost Converter, ripple.**

I. INTRODUCTION

In the present scenario, Uninterruptible Power Supply (UPS) systems are being widely used for computers, laptops, televisions, bio-medical equipments and telecommunication systems. The main requirement of these dc power supplies is that it should draw current with low harmonic content and also have power factor close to unity. The choice of the converter topology is important because it should result in the development of the power supply [1]–[3] with less compact, low cost and high efficiency.

The boost converter [4] – [5] has been generally used as a Power Factor Correction (PFC) converter, because of its simple circuit construction and high power handling capability which results in reduced harmonics content in input line currents, better utilization of power devices, lower conduction loss, lower input current ripple, improved power factor and better efficiency.

Due to the limitation of boost converter in terms of higher input current ripple, an interleaved boost converter topology is preferred for high-power applications [6]–[8] .But the application of hard switched technique, the switching losses are high resulting in reduced efficiency. Hence, a soft-switching interleaved boost converter [9]–[10] with ZVS and ZCS topology having higher efficiency, low component ratings, decreased switching losses, reduced size and cost of the components is discussed in this paper.

The power loss analysis of the DC-DC converters is carried out by estimation of losses [12]–[15] that includes device switching losses, inductor losses and diode losses. Then the efficiency [10], [11] and [16] of all the three DC-DC converter topologies are computed and their performance parameters are compared.

The organization of the paper is as follows: section II describes that how the DC–DC converters can be operated in continuous conduction mode (CCM). The section III explains about the ripple analysis of different topologies using Matlab simulations and the results are compared. The section IV deals about loss and efficiency evaluation.

II. CONVERTER TOPOLOGIES

(A) Boost Converter

A boost converter is a category of DC–DC converters called switch-mode converters which take a low voltage input and provide an output at a much higher voltage. The basic boost converter circuit consists of only a switch normally MOSFET, a diode, an inductor, and a capacitor. The input and output voltage relationship is controlled by the switch duty cycle.

The power stage can activate in continuous conduction mode (CCM), current flows in the inductor continuously during the complete switching cycle in steady-state operation. The continuous conduction mode of a boost converter assumes two states for each switching cycle. In the 'on' state, the transistor T_1 will be on and diode D_1 will be off. In the 'off' state, diode D_1 will be on. The duration of each state will vary.

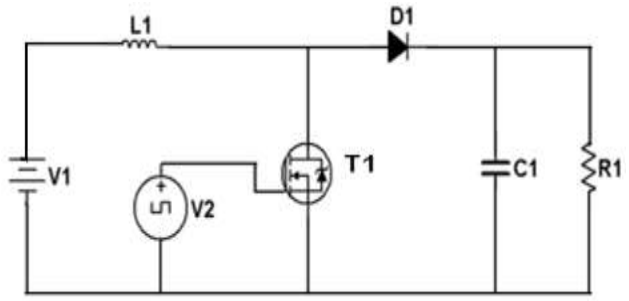

Fig. 1.Circuit Diagram of Boost Converter

The duration of the on state can be found using the expression

$$T_{on} = D \times T_s \quad (1)$$

In the expression, 'D' is the duty cycle. The duty cycle is set by the gate control circuit. The duty cycle is set by a ratio of the on time over the complete switching cycle denoted as T_s. The duration of the off state is expressed as

$$T_{off} = (1 - D) \times T_s \quad (2)$$

In the boost converter, the average output voltage is higher than the input voltage. When the switch is turned on, current through the inductor increases and the inductor starts to store energy. And when the switch is off, the stored energy in the inductor is dissipated to the load. The current is forced to flow through the diode and load during the turn off time. As a result the voltage across the load exceeds the source voltage.

The operation of the boost converter can be split into two modes namely mode 1 and mode 2. In mode 1, transistor T1 is switched on at time t = 0. The input current rises and flows through inductor L1 and transistor T1. In mode 2, transistor T1 is switched off at time t=t1. The input current now flows through L1, diode D1, C1 and load R1. The inductor current falls until the next cycle. The energy stored in inductor L1 flows through the load.

The major advantage of this topology is that the input current is continuous without additional filtering in the input.

(B) Interleaved Boost Converter

In the case of boost converter, ripples are present in the input current due to rise and fall of the inductor current. This problem can be reduced by using interleaved boost converter. The interleaved boost converter is shown in Fig.2.

The input current is the sum of two inductor currents I_{L1} and they are out of phase and tend to cancel each other. It is realized that the input ripple current is reduced compared to boost converter due to interleaving principle.

It is assumed that the inductance value of both inductors are L1 and L2, where L1= L2= L and the duty cycle of MOSFETs T1 and T2 denoted as TD1and TD2, with TD1=TD2=D.

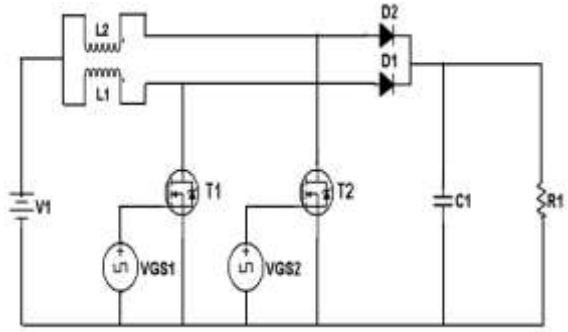

Fig. 2.Circuit Diagram of Interleaved Boost Converter

At the instant of time when, T1 is closed and T2 is opened. The current of the inductor L1 starts to rise, while inductor L2 continues to discharge. The rate of change of iLl is diLl /dt = Vi/L, while the rate of change of iL2 is diL2/dt = (Vi –Vo)/L. Following it, the MOSFETs T1 and T2 are opened; the inductors L1 and L2 discharge through the load. The rate of change of iL1 and iL2 are diLl /dt = diL2/dt = (Vi –Vo)/L. Then T2 is closed while T1 is still opened. The current of the inductor L2 starts to rise, while L1 continues to discharge. The rate of change of iL2 is diL2/dt = Vi/L, while the rate of change of iL1 is diLl /dt = (Vi –Vo)/L.T2 is opened and T1 is still opened. The inductors L1 and L2 discharge through the load. The rate of change of iL1 and iL2 are diLl /dt = diL2/dt /dt = (Vi –Vo)/L. Hence, IBC results in reduced input current and output voltage ripple.

(C) Soft Switching Interleaved Boost Converter

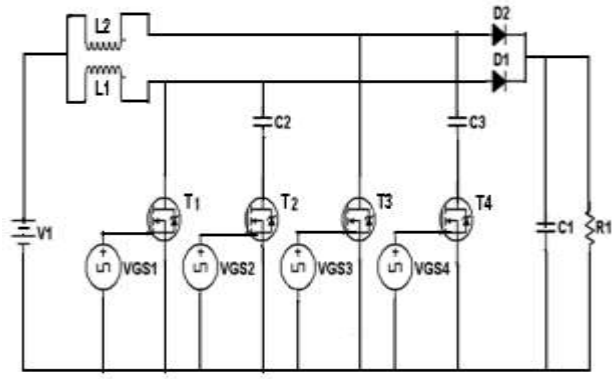

Fig. 3.Circuit Diagram of Soft Switching Interleaved Boost Converter

The soft switching DC–DC boost converter circuit consists of an Interleaved Boost Converters comprising of two main MOSFET switches and two auxiliary MOSFET switches as shown in Fig.3. The additional auxiliary circuits consist of MOSFET switches with snubber capacitors. The identically coupled inductors and identical diodes form a forward path and split the input currents equally to flow through the MOSFET switches to the load connected at the output. The turn–off switching losses of the main switches are reduced by using snubber capacitors in the auxiliary resonant circuits. In

this topology, the generation of switching losses is avoided by forcing voltage (ZVS) or current (ZCS) to zero during turn-on and turn-off of the switching actions of four MOSFET switches respectively.

At the instant of gate drive signals with desired duty cycle D = 0.78, applied to the main switches, transistors T1 and T3 are turned ON, the auxiliary switches T2 and T4 are turned OFF and the diodes D1 and D2 are reverse biased. The current through the coupled inductor increases and the inductors L1 and L2 starts to store up energy. Already stored energy from previous cycles in the output capacitor C1 discharges through the load. A delay is introduced into the gate drive signals applied to the auxiliary switches T2 and T4, so that there is a short commutation interval when all four transistors are turned ON. The snubber capacitors C2 and C3 tend to charge. The input current continuously rises and flows through coupled inductors and all transistors. The diodes D1 and D2 are reverse biased. The output capacitor C1 discharges continuously through the load.

After an interval of time, main transistors T1 and T3 are turned OFF, the auxiliary switches T2 and T4 are turned ON and the diodes D1 and D2 are forward biased. The load capacitor C1 and snubber capacitors C2 and C3 tend to charge. And when the main switches are made OFF, the stored energy in the inductor starts to dissipate. Because of high frequency switching nature, the converter is working in Continuous Conduction Mode (CCM). The current is forced to flow through the diodes and load during the turn off time of main switches. As a result the voltage across the load exceeds the source voltage.

TABLE I.

Simulation Parameters for Boost Converter Topologies

Component	Parameter
V_{in}(Input Voltage)	10.56
Switching Frequency	30KHz
Duty Cycle	0.78
V_{out}(Output Voltage)	48V
Output Current	2.5A
Output Power	120W
Boost Inductors L_1 and L_2	0.55mH
Snubber CapacitorsC_1 and C_2	5nF
Output Filter C_o	650μF
MOSFET ON-State Resistance R_{ON}	0.1 Ω
Diode ON-State Resistance R_D	0.05 Ω

III. RIPPLE ANALYSIS

The three different DC-DC converter topologies are modeled and simulated using Matlab/Simulink. The measured waveforms of voltage and current ripples with its percentage values are analyzed and the results are verified.

1. Boost Converter

The boost converter was simulated as per the mentioned specifications in Table1. The schematic diagram is illustrated in Figure 4.

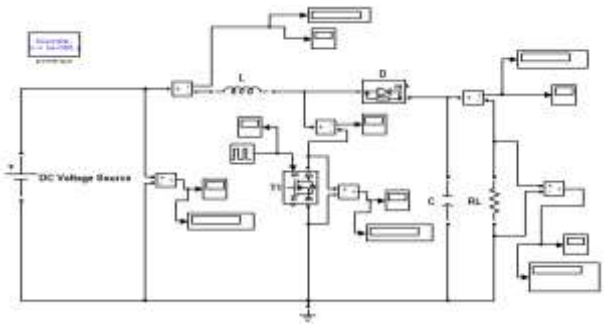

Fig. 4.Circuit Diagram of Simulation of Boost Converter

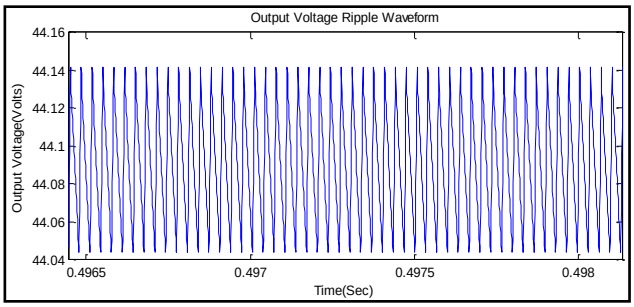

Fig. 5. Output Voltage Ripple waveform of Boost Converter

Output Voltage Ripple= 0.23 %

The converter has a simple structure and low cost. It is shown that the output voltage traces the dc input voltage in such a way that the ratio of the output voltage to the DC input voltage is always constant. The output voltage can be regulated to a voltage of 48V with the desired duty cycle of 0.78.

Also, it can be noted from this graph in Figure 5, that the output voltage ripple is reduced to very low percentage value to keep the output constant. As both the input and the output circuit share the single power switch, the switch stress is increased. In order to overcome this problem and to improve the efficiency of the converter, the interleaving technique can be used.

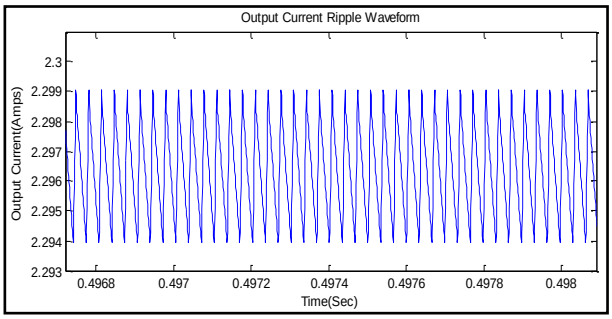

Fig. 6. Simulation Waveform of Output Current

Output Current Ripple= 0.22 %

It is observed that figure 6 illustrates that the output current with minimized current ripple.

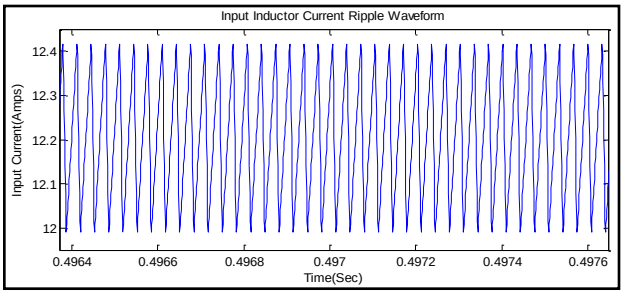

Fig. 7. Simulation Waveform of Input Inductor Current

Inductor Current Ripple = 3.28%

In order to optimize the converter performance by suitable selection of inductance in the input circuit, inductor current ripple is minimized and current waveform is given in Figure 7.

2. Interleaved Boost Converter

The interleaved boost converter is simulated and the simulink diagram is shown in figure8. The output voltage 48.062V is maintained constant as shown in figure9.

The figures 10 –14 illustrate clearly the voltage and current ripples waveforms. The voltage and current ripples are calculated in terms of percentage values.

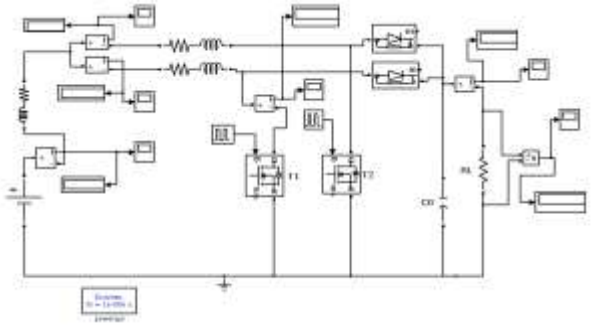

Fig. 8. Simulation Waveform of Interleaved Boost Converter

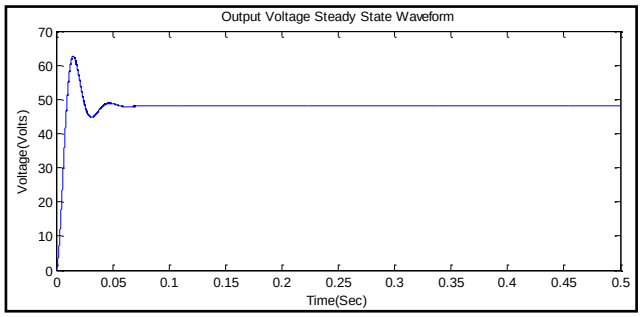

Fig. 9. Simulation Waveform of Steady State Output Voltage

Output Voltage= 48.062V

The duty cycle is only sensitive to the output voltage in CCM operation. In accordance to the duty cycle, the output voltage is maintained constant and the steady-state waveform is shown in Figure 9.

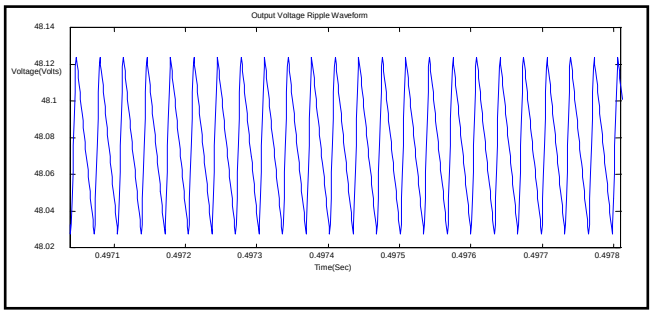

Fig. 10. Simulation Waveform of Output Voltage Ripple

Output Voltage Ripple= 0.18 %

The output voltage ripple is reduced dramatically to lesser extent and as shown in Figure 10.

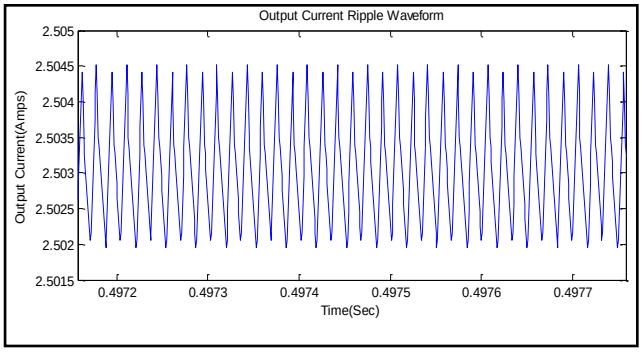

Fig. 11. Simulation Waveform of Output Current Ripple

Output Current Ripple= 0.1 %

For the constant input voltage and the required value of output capacitor maintained as per the circuit specifications, the output current ripple in the converter leads to a lower value and as shown in Figure 11.

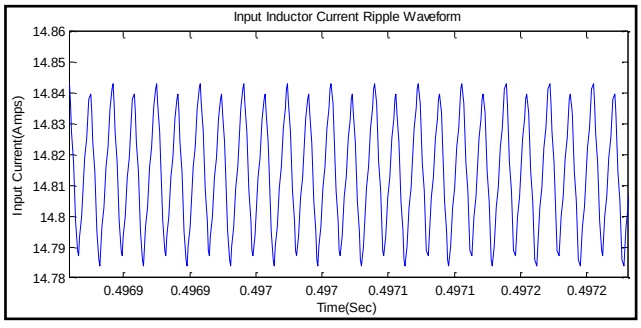

Fig. 12. Simulation Waveform of Input InductorCurrent

Inductor Current Ripple = 0.41%

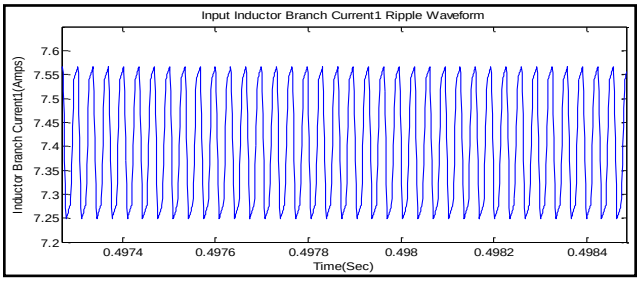

Fig. 13. Simulation Waveform of Input Inductor Branch Current IL1

Inductor1 Branch Current Ripple IL1 = 4.05%

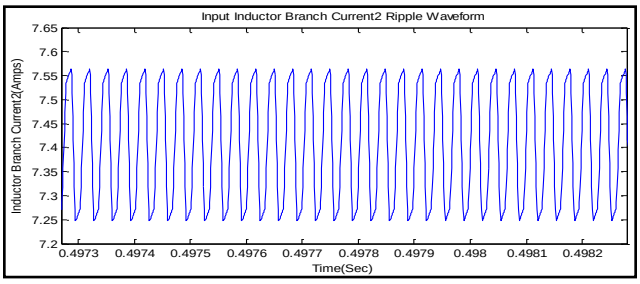

Fig. 14. Simulation Waveform of Input Inductor Branch Current IL2

Inductor2 Branch Current RippleIL2= 4.05%

In view of these simulation results from Figure 12, 13 and 14, the percentage of the input ripple current waveform is significantly reduced compared to the two independent inductors current ripple. Since the two phases of the circuit work with 180 degree phase shift, the input current ripple minimization is obtained at the desired duty cycle of D=0.78.

3. Soft Switched Interleaved Boost Converter

The soft switched interleaved boost converter is simulated as shown in Fig.15. The output voltage 48.03V is maintained constant as shown in figure16.

The figures 17 – 21 illustrate clearly the voltage and current ripple waveforms. The voltage and current ripples are calculated in terms of percentage values. The soft switched technique ensures low ripple.

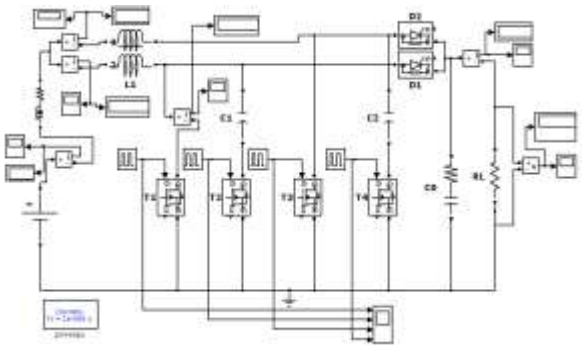

Fig. 15. Simulation of Soft Switched Interleaved Boost Converter

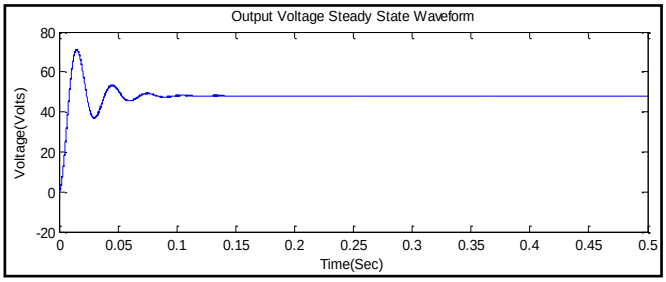

Fig. 16. Simulation Waveform of Output Voltage

Output Voltage= 48.03V

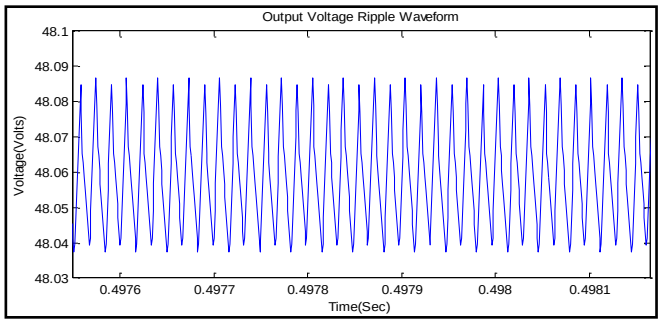

Fig. 17. Simulation Waveform of Output Ripple Voltage

Output Voltage Ripple= 0.1 %

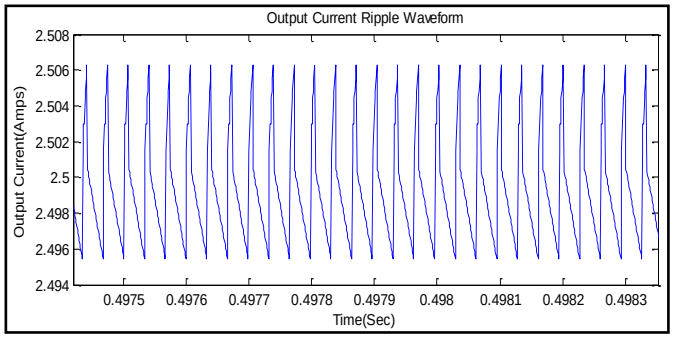

Fig. 18. Simulation Waveform of Output Ripple Current

Output Current Ripple= 0.36 %

The significant reduction in output current ripple due to fixed duty cycle and constant load is shown in Figure 18.

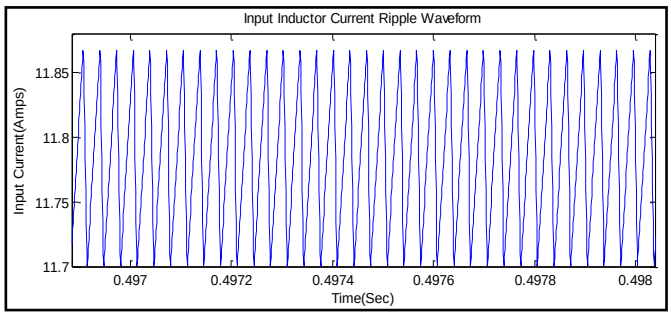

Fig. 19. Simulation Waveform of Input Inductor Current IL

Inductor Current Ripple = 1.36%

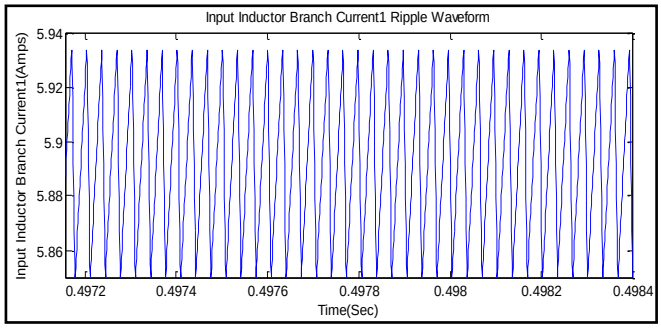

Fig. 20. Simulation Waveform of Input Inductor Branch Current IL1

Inductor1 Branch Current Ripple IL1 = 1.36%

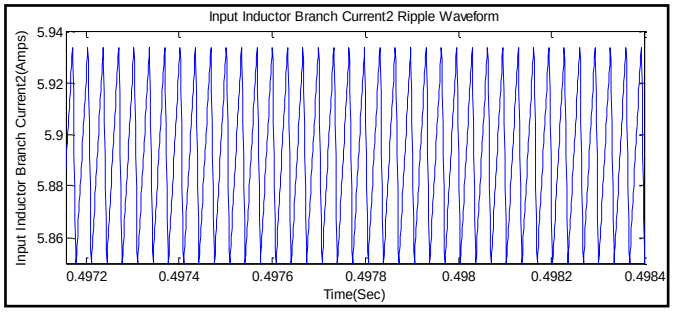

Fig. 21. Simulation Waveform of Input Inductor Branch Current IL2

Inductor2 Branch Current Ripple IL2 = 1.36%

Figs. 16-21 show the soft switched interleaved boost converter with reduced values of input current ripple, output voltage ripple and output current ripple. The ripple variations are very small at the desired duty ratio. The voltage stress on the main switches is shared by the effective auxiliary circuits.

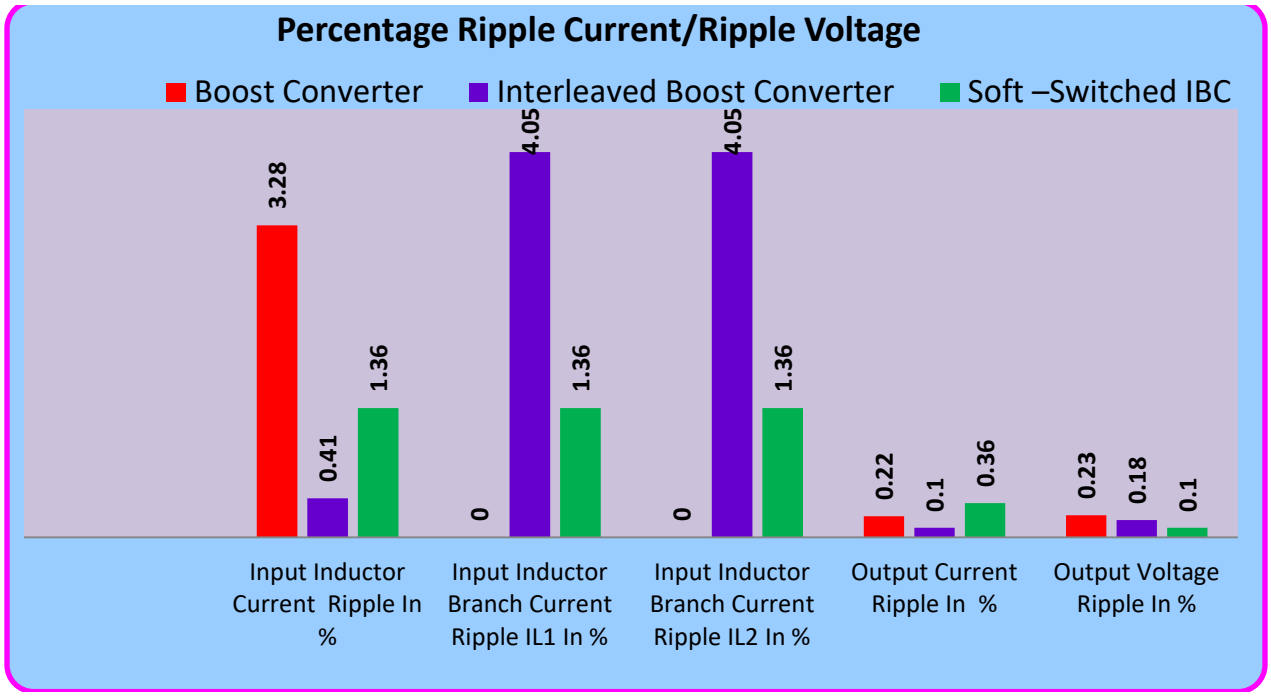

Fig. 22. Ripple Comparison Chart for Boost Converter Topologies

The ripple comparison chart for all the topologies is shown in Figure 22 and it indicates clearly that the soft switching interleaved boost converter has achieved lowest percentage value of input inductor current ripple and output voltage ripple among all other topologies.

IV. LOSS AND EFFICIENCY EVALUATION

A. *Component Losses*

There are four factors contribute to power MOSFET–related losses in a switching power converter.

1. *MOSFET– related switching losses:*

   a) *Conduction Losses:*

$$P_{Cond} = \left(I_{Drain} \times \sqrt{D}\right)^2 \times R_{DS-on} \qquad (3)$$

Where,

I_{Drain} = RMS value of drain current

D =Duty cycle for conduction

R_{DS-on} = On– State Drain–Source resistance

b) Switching Crossover Losses:

$$P_{Cross\ over} = \left(\frac{V_{DS}}{2}\right) \times I_{Drain} \times \left(t_{on} + t_{off}\right) \times f_S \quad (4)$$

Where,

V_{DS} = Drain – Source switching voltage

I_{Drain} = RMS drain current of MOSFET

t_{on} = Switch on–time

t_{off} = Switch off–time

f_s = Switching period frequency

c) Turn–on switching losses discharging the MOSFET output capacitance:

$$P_{Cout} = \frac{1}{2} \times C_{Oeq} \times V_{DS}^2 \times f_S \quad (5)$$

Where,

C_{Oeq} = Energy–related equivalent value for output capacitance integrated over the range from 0 V to 480 V.

d) The gate–driver power losses are:

$$P_{Gate} = Q_G \times V_{GS} \times f_S \quad (6)$$

Where,

Q_G is the MOSFET gate charge at the operating gate voltage VGS.

Q_G = 50 nC approximately

The total MOSFET loss is the sum of these four components:

$$P_{Total} = P_{Cond} + P_{Cross\ over} + P_{Cout} + P_{Gate} \quad (7)$$

2. DIODE– Related Losses:

The power losses of the diode PD consists of the reverse recovery losses P_{rrD} and the conduction lossesP_{CDD}.

$$P_D = P_{rrD} + P_{CDD} \quad (8)$$

The reverse recovery current is almost zero. Hence, P_{rrD} is zero.

The conduction losses P_{CDD} consist of the equivalent resistance losses P_{rD} and the forward voltage drop losses P_{fVD}.

$$P_{CDD} = P_{rD} + P_{fVD} \quad (9)$$

$$P_{rd} = I_{rms}^2 \times R_D \quad (10)$$

Where,

Irms =RMS value of diode current

R_D = Diode on– state resistance

$$P_{fVD} = V_f \times I_{avg} \quad (11)$$

Where,

V_f =Forward voltage drop across the diode

Iavg =Average value of diode current

3. INDUCTOR– Related Losses:

The power losses of the inductor consist of the core losses P_{fe} and the copper losses P_{cu}.

$$P_L = P_{fe} + P_{cu} \quad (12)$$

The core losses P_{fe} can be calculated as

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c l_m \quad (13)$$

Where,

K_{fe} = Constant of proportionality

ΔB = Peak ac flux density

β = 2.6

A_c = Core cross sectional area

l_m = Core's mean magnetic path length

The Peak ac flux density ΔB is calculated as

$$\Delta B = \frac{V_{in} D T_s}{2 n A_c} 10^4 \quad (14)$$

Where,

V_{in} = Converter input voltage

D =Desired duty cycle

T_s =Switching period

n = Number of turns in inductor windings

A_c = Core cross sectional area

The copper losses P_{cu} can be calculated as:

The conductor losses in an inductor are due to DC copper losses $P_{L\text{-}DC}$ and AC copper losses.

The DC copper losses are estimated by

$$P_{L-DC} = I_{L-rms}^2 . R_{DC} \quad (15)$$

Where,

I_{L-rms} = RMS value of inductor current

R_{DC} = DC resistance of the inductor

The AC copper losses are estimated by using the calculated value of DC resistance and the AC resistance multiplying factor, MR, obtained from the AC resistance curves, power loss in the winding can be calculated as

$$P_{L-AC} = I_{L-rms}^{2} \cdot R_{AC} \quad (16)$$

Where,

I_{L-rms} =RMS value of inductor current

R_{AC} = AC resistance of the inductor

The boost converter introduces increased EMI due to high di/dt which in turn will increase input inductor ripple current and leads to higher inductor and switching power losses. These losses significantly degrade the efficiency of the converter. But, the interleaved boost converter introduces 180° phase shift and results in less input current ripple. It also reduces output ripple current. Hence, the total losses are reduced compared with boost topology.

Efficiency

Efficiency can be defined as the ratio of output power delivered to load to the input power supplied to the converter.

Mathematically, it is calculated as,

$$\eta = \frac{P_{i/p} - P_{loss}}{P_{i/p}} \times 100 \quad (17)$$

Where,

η =Efficiency of the converter

$P_{i/p}$ =Total input power to the converter

P_{loss} =Total component losses of the converter

Figure 23 shows the different topologies of DC– DC boost converters efficiency for the same input voltage, same duty cycle with constant load and at the following test conditions: fsw = 30 kHz, Vin = 10.56V, D = 0.78 and Vo =48V. The efficiency improvement comes mostly due to the reduction of the component losses. As it can be seen, for soft switched interleaved boost converter the maximum efficiency of 93.2% is reached with constant output voltage. The effective soft switched IBC efficiency is increased by about 17.64%, which does a significant improvement over the conventional boost converter.

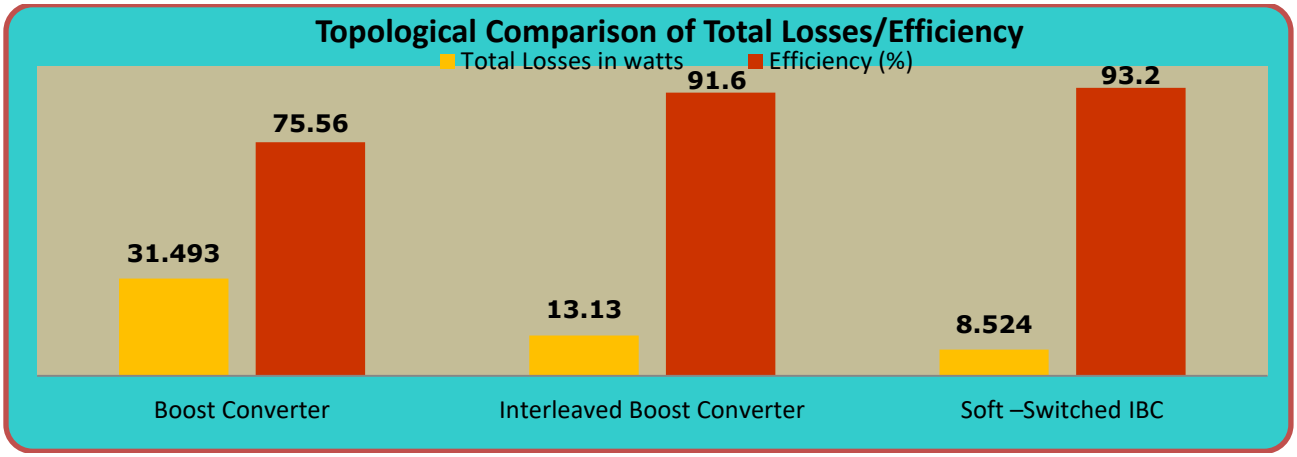

Fig. 23. Comparison Chart for Total Losses / Efficiency in Boost Converter Topologies

V. CONCLUSION

In this paper, the three different DC – DC boost converter topologies are discussed and its performance characteristics in terms of ripple, component power losses and efficiency are investigated. The proposed soft switched interleaved boost converter shows a high efficiency. The ZVS at turn on and ZCS at turn off soft-switching performance are achieved for both the main and auxiliary switches which reduce the switching losses. The voltage stress on the main switches is shared by the effective auxiliary circuits. The proposed soft–switched converter operating in the continuous conduction mode (CCM) proves to be an excellent candidate topology for obtaining lesser ripples with low power losses attributing high efficiency. Moreover, it is suitable for delivering constant output voltage for telecommunication system.

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