Static - CMOS Technology Based Low Power Carry Look Ahead Adder for High Speed Applications

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Abstract: **A logic design whose outputs at a specified time are a function only of the inputs at that time. In practice, any combinational circuit will have a finite transit time, or delay, between the inputs changing; the motive of the term combinational is to include algebraic elements i.e, AND gates, OR gates, etc. and preclude memory elements i.e flipflops, etc. Carry-look ahead adder is a method that is used in multibit parallel adders whereby the carry into an individual elements of the adder can be predicted with a smaller delay than that required for the carry to be produced by transferring through previous adder stages as a result of adding the less significant addend and augend bits.**

***Key Words*: Half Adder, CMOS, Tanner EDA, Logic Design Static, Ripple Carry Adder, Carry Look Ahead Adder, Multisim, Xilinx**

I. INTRODUCTION

In digital circuit theory, combinational circuits which is also called as time independent logic is a type of digital logic which is implemented by Boolean circuits in which the output is the pure function of the input. A digital logic called the carry-look ahead adder or fast adder is a type of adder which improves speed by reducing the amount of time required to determine carry bits. The advantages of carry-look ahead adder is that it has reduced propagation delay and it has faster addition logic. The disadvantages of carry-look ahead adder circuit is the circuits gets complicated if the number of variables increase and the circuit is costlier as it demands more number of hardware. To reduce the computation time, two binary numbers can be added using carry-look ahead adders. They work by creating two signals P and G known as the Carry Propagator and Carry Generator. The carry propagator is introduced to the next level whereas the carry generator is used to consolidate the output carry, regardless of input carry. The circuit of full adder is used to find the number of gate levels for the carry propagation. The signal from the input carry Cin to output carry count requires and AND gate and an OR gate, which constitutes two gate levels.

II. EXISTING SYSTEM

A full adder is a digital circuit that performs logical operations like addition. The main difference between half adder and full adder is that the full adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry and it is named as Cin. The outputs are sum and carry. The output sum is an EXOR between the input A and the half adder sum output with B and Cin inputs. We must also know the fact that the Cout will be true if any of the two inputs out of the three are HIGH. A ripple carry adder is a logic circuit in which the carry out of each full adder is the carry in of the next full adder. Each carry bit is rippled into the next stage. Sum and carry of the full adder 1 is valid only after the propagation delay of Full adder 1. In the same way sum s3 of the full adder 4 is valid only after the joint propagation delays of full adder 1 to full adder 4.The propagation delay is reduced by carry look ahead adder by introducing more complex hardware. From the Boolean equations we can observe that C4 does not have to wait for C3 and C2 to propagate but actually C4 is propagated at the same time as C3 and C2.They work by creating two signals P and G known to be Carry propagator and Carry Generator. Carry look ahead are designed using multisim ,tanner and Xilinx

Two binary inputs and two binary outputs are required by half adder circuits. The input variables designated the augends and added bits; the sum and carry are produced by the output variables.

Fig-1.1: Block diagram of Half Adder

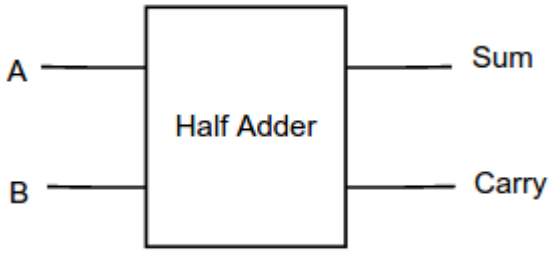


Fig-1.2: Block diagram of Full Adder

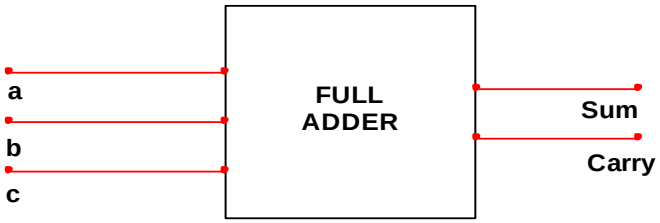
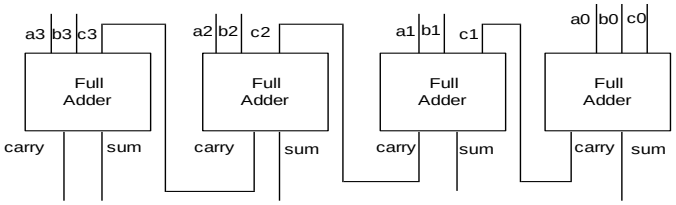


Fig-1.3: Block diagram of Ripple Carry Adder

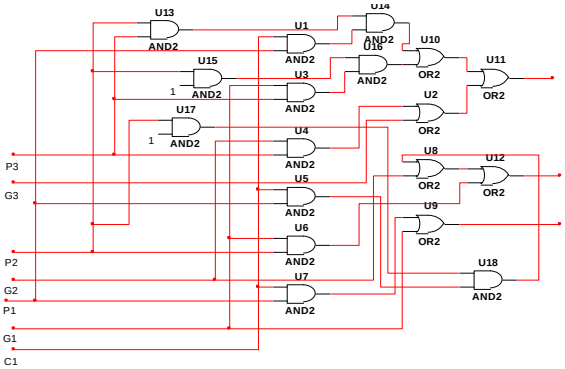


From fig 1.3 the sum S3 is produced by the corresponding full adder as the input signals are applied to it . But the carry input C3 is not available on its steady state value until carry C2 is available at its steady state value. Similarly C2 depends on C1 and C1 depends on Cin. Therefore carry must propagate to all the stages in order that output S# and carry C4 settle their final steady state value. Hence the propagation time is equal to the propagation delay of the typical gate and the number of gate levels in the circuit. For example if the full adder stage has a propagation delay of 20n seconds, then S3 will reach its final correct value after 60n (20*3) seconds. If we extend the number of stages for adding more number of bits which makes the situation much worse.

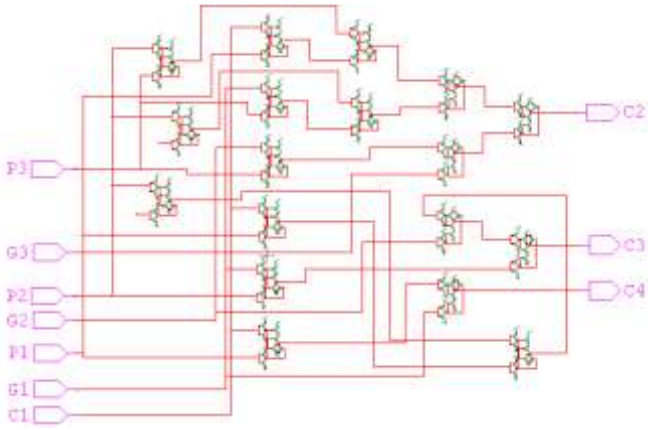
IV. CARRY LOOK AHEAD ADDER

Carry Look Ahead adder is made up of multiple number of 'AND' gates as well as 'OR' gates. Results waveforms of normal logic diagram of carry look ahead adder and CMOS design of carry look ahead adder are compared The Kogge stone adder and the Brent Kung adder are the examples of carry look ahead adder. In case of parallel adders, the bits of augend and addend must be available at the same time to perform the computation of addition of two binary numbers. In a parallel adder circuit the carry output of each adder is connected to the carry input of the next adder and hence it is also called as ripple carry type adder. In such adders it is impossible to produce the sum and carry outputs until the input carry occurs. This causes a delay called carry propagation delay in which there will be considerable time delay in the addition process. In any combinational circuit, the gates should be penetrated by the signals before the correct output sum is available in the output terminals.

[1]Logic Diagram of Carry Look Ahead Adder



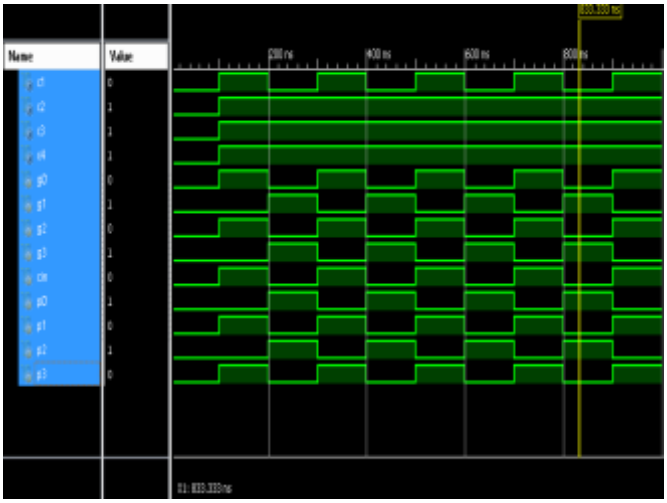
[2]CMOS Design of Carry Look Ahead Adder



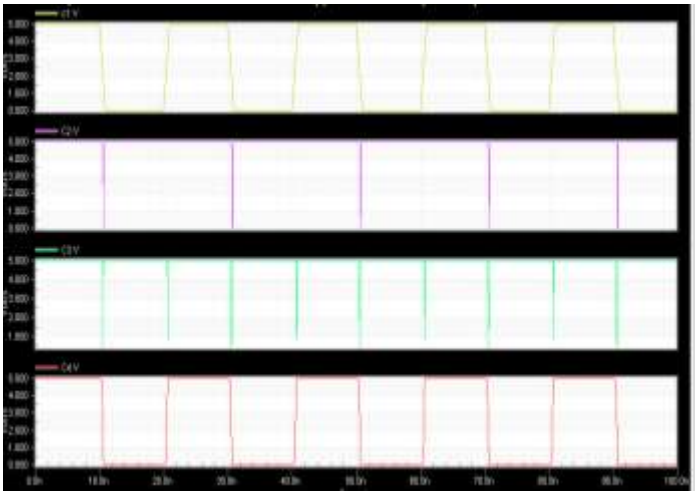
V. RESULTS

B.1 OUTPUT:

Waveform of Logic design of Carry Look Ahead Adder:



Waveform of CMOS design of Carry Look Ahead Adder:



VI. CONCLUSION

It has been observed from the simulation results that performance of adder architectures varies with various CMOS design. The output of these two designs of Carry Look Ahead Adders are same. The current fabrication size of Carry Look Ahead adder is 125nm.If the fabrication size reduced to less than 100nm, the adder performance varies and can be absorbed using static (CMOS) technology. From this research the (CMOS) can be achieved by operating0 point within 0.9v.This research is very useful and more advantageous in microprocessor industries. This shows that the speed at which the number of bits added in the parallel adder depends on the carry propagation time. However the gates are propagated by the signal at a given enough time to produce the correct or desired output. There are two methods to get high speed in the parallel adder to produce binary addition..By employing faster gates with reduced delays, the propagation delay is reduced. But there will be a capability limit for every logic gate. The other way is to increase the circuit complexity inorder to reduce the carry delay time. There are several methods to speed up the parallel adder, one commonly used method employs the principle to eliminate inter stage carry logic is by look ahead carry addition.

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