A Wide-band CMOS Low Noise Amplifier for LTE Application

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***Abstract*—A wideband Low Noise Amplifier is designed for Long term Evolution (LTE) application. A common source configuration with a resistive shunt feedback which is used to provide wide band input matching and to obtain lower noise figure. The proposed LNA is designed in 0.13µm technology. After the simulation, design consumes 110.6mA of current from 2.5V supply which operates on frequency of 0.7GHz to 2.7GHz. The simulations such as (S11=S22)>-10dB, S21=25dB show that all the parameters are working in appropriate manner.**

***Keywords*—LNA, LTE, CMOS, Low Noise, Wideband**

I. INTRODUCTION

LNA is a part of satellite communication system which is typically a first stage at the receiver side. Incoming signal from satellite has to be amplified but without introducing much noise. So important parameters while designing a LNA are its noise figure and gain. The design of a LNA determines the sensitivity and noise level of the receiver side. Our system is specifically designed for Long term Evolution (LTE) technology. Since it is the first block at the receiver, it has to provide high linearity and flat gain for the entire band of frequency. In order to reduce the size of the chip, we have used TSMC 0.13µm technology.

Review of existing wide band LNA techniques:-

In earlier projects, common gate configurations were used. Since all the projects are focused mainly towards minimizing noise figure, their gain and reflection figures are not up to the mark. Common gate configuration is mainly used for dealing with the high frequency. In CG configuration, source has very low impedance, which is certainly not desired. To eliminate the effect of low impedance, cascode setup is used which uses relatively high supply voltage. Their resulting noise figure is <3.5dB and gain value is 25dB. Even though we have used CS configuration, we have managed to obtain values more or less the same as of their values.

Proposed System:-

i. Biasing –

As per CMOS technology standard, maximum gate supply should be 2.5V and maximum drain supply should be 3.3V. Appropriate voltage supply for the proposed system is 0.7V for gate supply and 2.5V for drain supply and these values are obtained by doing DC analysis as well as fine tuning. A resistor R2 and a capacitor C3 is added between gate supply and gate terminal. Capacitor C11 is connected in parallel and grounded to restrict the reverse current and resistor is used as a part of biasing technique. Inductor C11 is used at the drain since inductor provides high bandwidth.

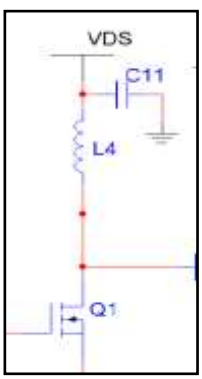

Fig.1

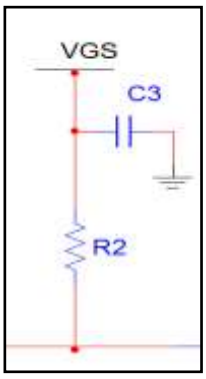

Fig. 2

ii. Design of impedance matching –

Input and output impedance is matched to its signal source to maximize the power transfer. A properly matched circuit is used to minimize signal reflectionfrom the load. Since the filters are less bulky and can be effectively used for wideband application, low pass filters are used. In the proposed system, input and output matching circuits are designed by taking smith chart into consideration. The resistive shunt-feedback topology has been extensively used because of its superior broadband characteristics. Applying shunt feedback to a CS amplifier allows the amplifier to be matched over a broad bandwidth while having minimal impact on the noise figure. Presence of feedback resistor may degrade the noise depending on the value of resistor.

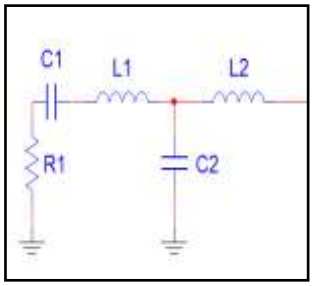

Fig. 3A

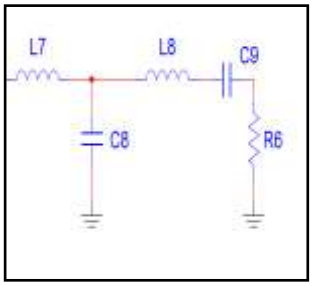

Fig. 3B

Simulation Results:

A wideband CMOS LNA is simulated with 'Advanced Design System' software using 0.13µm technology. The design is targeted to achieve low noise figure and higher gain across the specified bandwidth (0.7 to 2.7GHz).Fig. 4.A shows the simulated result of voltage gain in the required frequency band.

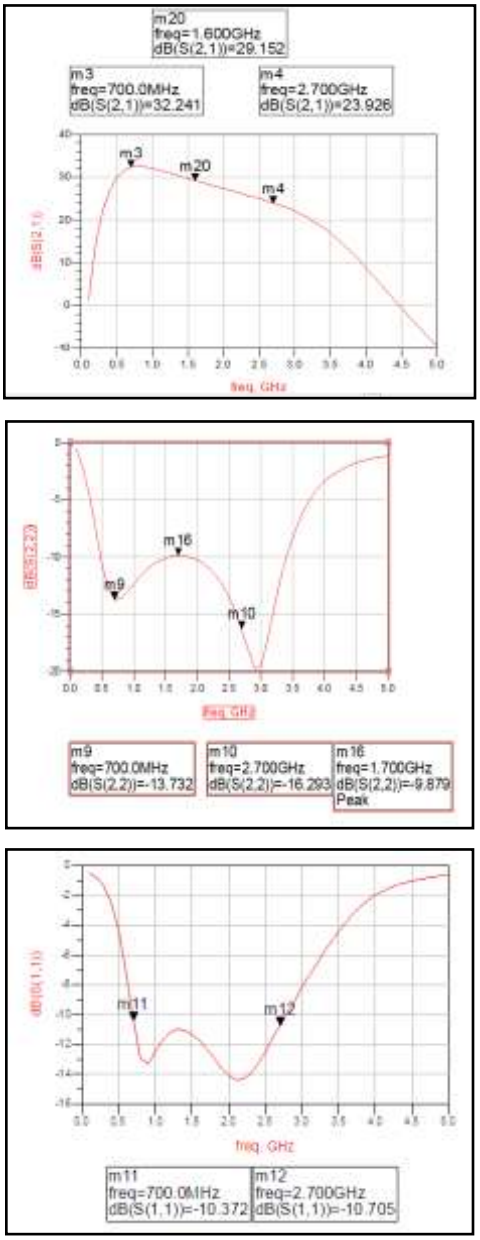

Fig. 4A, 4B and 4C

As per objective of the system, gain is achieved above 17dB and noise figure near to 3dB over the band. Also, proposed LNA achieves S11=S22 > -10dB which validates input and output matching. Fig.4.B and fig.4.C shows input and output reflection coefficients of the designed system respectively.

Table 1shows performance parameter comparison of previous referred papers.

LNA	CMOS Technology	Bandwidth (GHz)	Gain(Av)	Noise Figure
1	0.18 µm	0.5-3.5GHz	17dB	2.5dB
2	0.18 µm	0.7-2.7GHz	17dB	<2.5dB
This Work	0.13 µm	0.7-2.7GHz	25dB	3dB

Table 1

Layout:

Dimension of layout of proposed system is (1010.9 µm * 1041.12µm).Fig 5 shows layout proposed system.

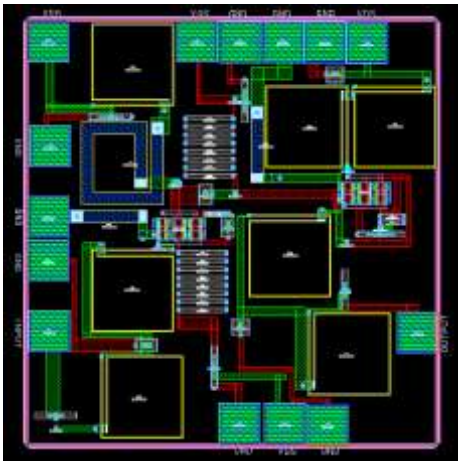

Fig. 5

II. CONCLUSIONS

The proposed LNA is capable of working in next level standards like LTE, etc. The LNA operates in frequency band of 0.7 GHz to 2.7 GHz which is designed in 0.13µm CMOS technology. High pass filters are used to achieve matching without degrading noise figure. Simulated noise figure is approximately 3dB where input and output reflection coefficients are below -10dB. The voltage gain i.e. S21 is between 23 to 30dB across the bandwidth.

ACKNOWLEDGMENT

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REFERENCES

[1]. O.A.Hidayov, N.H. Nam, G. Yoon, S.K. Han and S.G. Lee:' 0.7–2.7 GHz wideband CMOS low-noise amplifier for LTE application' (ELECTRONICS LETTERS 7th November 2013 Vol. 49 No. 23 pp. 1433–1435).

[2]. Olim Hidayov, Il Hoon Jang, Seok Kyun Han, and Sang-Gug Lee, Justin Cartwight:' A Wide-band CMOS Low Noise Amplifier for LTE Application'.

[3]. Wei-Rern Liao, Jeng-Rern Yang:' A 0.5-3.5GHz Wideband CMOS LNA for LTE Application'.