Review Paper on Design and Implementation of Kogge-Stone Adder Using Cadence Virtuoso

Alfiya Kouser[1], Harshitha D[2], Karotiya Rishabh[3], Lakshmi Narsimha[4], Prof. Tanya Mendez[5]
[1,2,3,4]*UG Students, Department of Electronics and Communication Engineering, AIET, Mijar, Moodbidri, Karnataka, India*
[5]*Department of Electronics and Communication Engineering, AIET, Mijar, Moodbidri, Karnataka, India*

***Abstract*—In Very Large Scale Integration (VLSI) designs, Parallel Prefix Adder (PPA) have better delay performance. A parallel prefix adder involves the execution of the operation in parallel which can be obtained by segmentation into smaller pieces. The binary addition is the basic arithmetic operation in digital circuits and it is essential in most of the digital systems including Arithmetic and Logic Unit (ALU), Microprocessor and Digital Signal Processors (DSP). At present, the research continues in increasing the adder's delay performance. In this paper the investigation of Kogge Stone Adder (KSA) using Carry Look-ahead Adder (CLA) is done. These adders are implemented using Cadence Virtuoso Platform in both the front-end and back-end design.**

***Keywords*-PPA, ALU, KSA, CLA**

I. INTRODUCTION

Binary adders are one of the essential and broadly utilized arithmetic operation in current Integrated Circuits (IC's). They tend to play a critical role in determining the performance of the design. Arithmetic operation is the normal regular task in advanced incorporated circuits. The least complex circuit includes addition, **subtraction** and multiplication or divisions. The computation should be fast and the area consumed by the computation should be fast and the power consumption should be less. These are the essential necessities for any adders. Parallel processing is a type of calculation in which numerous figuring are done at the same time, working on the rule that substantial issues can regularly be separated into simpler ones, which are then settled simultaneously in parallel. These are a few unique types of parallel registering bit level, instruction level, data, and task parallelism. Parallelism has been utilized power consumption and consequently heat generation by computers has become a major concern in recent years, parallel computing has become the dominant paradigm in computer architecture, mainly in the form of multi-core processors.

Parallel computers can be roughly classified according to the level at which the hardware supports parallelism, with core and multi-processor computers having multiple processing elements within a solitary machine. Area and time devoured by the circuit are the essential critical prerequisites. Numbers can be spoken to in advanced circuits in different ways. Thus, developing efficient adder architecture is crucial to improving the efficiency of the design. Carry Look-ahead Adder are based on the parallel prefix computation. After many years of research, focus is on improving the delay performance of the adder.

II. LITERATURE REVIEW

Penchalaiah and Kumar [1] did research on a new PPA architecture called KSA which was proposed for 8, 16, 32 and 64-bit addition. The proposed method was implemented and the results were validated by the comparison of KSA with CSKA in terms of area, delay, speed and power consumption. The obtained results on the proposed KSA reported the minimum energy consumption compared with the CSKA along with area compaction and high speed. The proposed method can be very useful in high speed applications.

Hoe et al. [2] has proposed three types of carry-tree adders (the Kogge-Stone, sparse Kogge-Stone, and spanning tree adder) and compares them to the simple Ripple Carry Adder (RCA) and Carry Skip Adder (CSA). These designs of varied bit-widths were implemented on a Xilinx Spartan 3E FPGA and delay measurements were made with a high-performance logic analyzer. Due to the presence of a fast carry-chain, the RCA designs exhibit better delay performance up to 128 bits. The carry-tree adders are expected to have a speed advantage over the RCA as bit widths approach 256. Hence it is concluded that the carry-tree adders eventually surpass the performance of the linear adder designs at high bit-widths, expected to be in the 128 to 256 bit range.

Shilpa C. N et al. [3] worked on the design and performance of the Kogge Stone Parallel Prefix Adders and implemented it using different design technique. CMOS (Complementary Metal Oxide Semiconductor) and GDI (Gate Diffusion Input) are the different design technique used. The design and simulation of logic gates were performed on CADENCE Design Suit 6.1.6 using virtuoso and ADE Environment at GPDK 180nm technology. The execution measurement considered for the performance of the KSA is delay, number of gate count/Transistor Count (area) and power. Simulation studies are done for 4-bit, 8-bit and 16-bit input data. The results of the comparative analysis, showed how the performance can vary from 4 bit to 16 bit adder architecture.

Gurkaynak et al. [4] had described the design of radix-3 and radix- 4 parallel prefix adders, the main building blocks of the higher radix parallel prefix adders were identified and higher radix structures of Kogge-Stone Adders were presented. Work showed that the logic depth could be reduced by 50% and the cell count can be reduced as much as 47% for 64-bit adders. Simulation results indicated that radix-4 adders could be 30% more faster than radix-2 realizations. It was also noted that the proposed architectures not only reduced the depth of the carry propagation network as much as 50%, but the number of cells required also decreased by as much as 47% (for the Radix-4 Kogge-Stone adder) when compared to the Radix-2 realizations.

Penumutchi et al. [5] worked on the GDI technique to design the circuits for high speed and low power applications. A 64 bit GDI logic based KSA schematic was designed using MENTOR GRAPHICS EDA Tool in 130nm Technology. Performance parameters like delay and average power consumption (at various dimensions of MOS transistors and over a range of supply voltages) were measured and the best adder in terms of performance was observed as the one with a delay of 407.07ps designed in GDI Technique. When compared to the others, Kogge -Stone Adder was identified as the fastest adder and also had a lower fan-out at the output which increased its performance but on the other hand, it occupied much area and created wiring congestion problems. Much more advanced tool support was required to design KSA with the exact expected performance.

K. Swetha et al. [6] proposed the fastest adder and used in many data processing applications to perform the fast arithmetic functions. The speed of operation of the CSLA is limited by the time required to propagate a carry through the adder. The implementation of 16-bit Linear Carry Select Adder (LCSLA) with Kogge Stone Adder (KSA) was prepared in terms of Binary to Excess-1 converter (BEC) and extra logic gates. A high speed adder was designed by merging the CSLA and KSA algorithms instead of using ripple carry adder (RCA) and due to that the delay is reduced, but it occupied more area. Synthesis and simulation result of CSLA with KSA was done by using Xilinx ISE 13.3 and Cadence EDA tool and compared interms of ADP and PDP, which showed that 16-bit adder with FCL for KSA with BEC based CSLA for Cin=0 **affords** better performance in terms of ADP and PDP and it had 2% efficiency in ADP and 7% efficiency in PDP than other methods.

Yezerla and Rajendra [7] proposed their design and implemented using Xilinx vertex 5FPGA and the adder delays were estimated using Agilent 1692A logic analyzer. The 16-bit SKA (Sparse Kogge Stone Adder) computes the carries with Black Cells (BC's) and Grey Cells (GC's) and terminates with a 4-bit RCA (Ripple Carry Adder). The 16-bit STA (Spanning Tree Adder) used also terminates with RCA and uses BC's and GC's and full adders but has difference in the interconnection between them. The 16-bit KSA (Kogge Stone Adder) design used 16-bit BC's and 15 GC's with less delay compare to SKA and STA. The 16-bit BKA (Brent Kung Adder) used 14 BC's and 11 GC's which is less compared to KSA and hence has less architecture and occupies less space than KSA. The delay measurement shows that SKA and BKA have almost same delay whereas STA has better delay results. The efficiency has increased for delay up to 5.77% for RCA and for KSA has improved by 19.28%.

Athira et al. [8] proposed a Kogge-Stone Adder (KSA) with low power consumption and delay. Usually, Ripple Carry Adders (RCA) are preferred for addition of two N-bit numbers as these RCAs provide faster design time among all types of conventional methods. However, RCA's have limitation that every full adder block must wait till carry bits were generated from previous blocks of the full adder. The implemented Kogge-Stone Adder was a parallel prefix form Carry Look Ahead (CLA) adder. Parallel prefix adders (PPA) are tree based structure which speed up the binary addition. Hence prefix adders are used for fast addition algorithms. The experimental result shows that the addition by using Kogge-Stone Adder reduces power consumption and delay in comparison with other conventional logics. The performance analysis was based on the power consumption and the worst case delay in performing the operation. The CMOS adders were realized using TSMC 45 nm technologies. The results showed that the proposed KSA greatly reduces the power consumption.

Daphni and Vijula Grace [9] clarified about the design and analysis of various Parallel Prefix Adder (PPA) and compared the performance of these adder on the aspects of area, delay and power. From the investigation results it was clear that the Kogge stone adder (KSA) was superior for the delay process, so the speed of the addition was automatically increased. But it takes more power consumption and area. In addition to that it is described the comparison of PPA with the performance on the aspects of area, power and delay. From the reviewed analysis results it was clear that the KSA was better for the delay process, so the speed of the addition was automatically increased. But it takes more power consumption and area. Newer implementation can focus on attaining better area-power delay PPA for low power VLSI applications.

Smith and Chew Lim [10] introduced two innovations in the design of prefix adder carry trees which used high-valency prefix cells to achieve low logical depth and end-around carry adders with reduced fan-out loading (compared with the carry select and fagged prefix adders). An algorithm for generating parallel prefix carry trees suitable for use in a VLSI synthesis tool was presented with variable parameters including caw tree width, prefix cell valency, and the spacing of repeated carry trees. The area-delay design space was mapped for a 0.25pm CMOS technology. An algorithm for generating parallel prefix trees with variable parameters was introduced and the

performance results derived from SPICE simulations using a uniform sizing model have been presented.

III. CONCLUSION

The primary purpose of the paper is to make a survey of all the details and parameters of the Parallel Prefix Adder, Ripple Carry Adder, Carry Skip Adder Carry, Look Ahead Adder and Brent-Kung adder in order to identify the efficient adder in terms of delay and power consumption. The survey results concludes that Kogge-Stone Adder reported the minimum energy consumption when compared with other adders and also showed the performance analysis of 4-bit and 16-bit adder architecture, and performance based on ADP and PDP.

REFERENCES

[1]. U. Penchalaiah and V.G. Siva Kumar "Design of High-Speed and Energy-Efficient Parallel Prefix Kogge Stone Adder", IEEE 2013.
[2]. David H. K. Hoe, Chris Martinez and Sri Jyothsna Vundavalli "Design and Characterization of Parallel Prefix Adders using FPGAs", IEEE 2011.
[3]. C. N. Shilpa, Kunjan D. Shinde, H. V. Nithin, "Design,Implementation and Comparative Analysis of Kogge Stone Adder using CMOS and GDI design:A VLSI Based Approach", IEEE 2016.
[4]. FrankK. Gurkaynad, Yusuf Leblebicit, Laurent Chaouatt and Patrik J. McGuinnessz "Higher Radix Kogge-Stone Parallel Prefix Adder Architectures", IEEE 2000.
[5]. Bujjibabu Penumutchi, Satyanarayana vella, Harichndra prasad satti, "Kogge Stone Adder with GDI Technique in 130nm Technology for High performance DSP Applications", IEEE 2017.
[6]. Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, "Electron spectroscopy studies on magneto-optical media and plastic substrate interface," IEEE Transl. J. Magn. Japan, vol. 2, pp. 740–741, August 1987 [Digests 9th Annual Conf. Magnetics Japan, p. 301, 1982].
[7]. Sudheer kumar yezerla,B Rajendra, "Design and estimation of delay,power and area for parallel prefix adders", IEEE 2014.
[8]. T. S. ATHIRA, R. DIVYA, M. KARTHIK, A. MANIKANDAN, "DESIGN OF KOGGE-STONE FOR FAST ADDITION", International Journal of Industrial Electronics and Electrical Engineering, ISSN: 2347-6982 Volume-5, Issue-4, Apirl-2017.
[9]. S. Daphni and K. S. Vijula Grace, "A REVIEW ANALYSIS OF PARALLEL PREFIX ADDERS FOR BETTER PERFORMNCE IN VLSI APPLICATIONS", IEEE International Conference on Circuits and Systems (ICCS) 2017.
[10]. Andrew Beaumont-Smith and Cheng-Chew Lim, "Parallel Prefix Adder Design", IEEE 2001.