Implementation of a 7-segment Display on BASYS3 Board

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Abstract: **The paper presents a simple design and implementation of a Seven-Segment Displays Designs on BASYS3 Board.The purpose of this paper to practice implementation VHDL codes and performing simulations on various counter designs and implement designs on FPGA with BASYS3 board utilizing switches, LEDs, and seven-segment displays. In this paper we are going to use Pmod KYPD: 16-button Keypad. This keypad has 16 keys and they are arranged in an array of 4 rows and 4 columns. This keypad can be attached to one of the Pmod ports of FPGA board. On BASYS 3 we have 3 such ports, JA, JB and JC. Out of 12 pins, 8 are used for data and 4 for power supply.**

Keywords: **BASYS 3 board, Pmod KYPD, Seven-Segment Displays, USB cable, PC**

I. INTRODUCTION

The **V**ery High Speed Integrated Circuit **H**ardware **D**escription **L**anguage (VHDL) modeling language supports three kinds of modeling styles: dataflow, structural and behavioral. Dataflow and structural modeling are used to model combinatorial circuits whereas behavioral modeling is used for both combinatorial and sequential circuits. This paper illustrates the use of all three types of modeling by creating simple combinatorial circuits targeting BASYS-3 board and using the Vivado software tool.

II. HARDWARE COMPONENTS

A. BASYS3 Board

The BASYS3 board is a complete, ready-to-use digital circuit development platform based on the latest Artix-7 Field Programmable Gate Array (FPGA) from Xilinx. With its high-capacity FPGA (Xilinx part number XC7A35T-1CPG236C), low overall cost, and collection of USB, VGA, and other ports, the BASYS3can host designs ranging from introductory combinational circuits to complex sequential circuits like embedded processors and controllers. It includes enough switches, LEDs and other I/O devices to allow a large number of designs to be completed without the need for any additional hardware, and enough uncommitted FPGA I/O pins to allow designs to be expanded using DigilentPmods or other custom boards and circuits [1]. The Basys3 board is shown in Fig. 1. The Basys3 board has the following components:

- 1,800 Kbits of fast block RAM
- 33,280 logic cells in 5200 slices (each slice contains four 6-input LUTs and 8 flip-flops)
- Five clock management tiles, each with a phase-locked loop (PLL)
- Internal clock speeds exceeding 450MHz
- 16 User Switches
- 16 User LEDs
- 5 User Pushbuttons
- 4-digit 7-segment display
- Three Pmod connectors
- Pmod for XADC signals
- Serial Flash

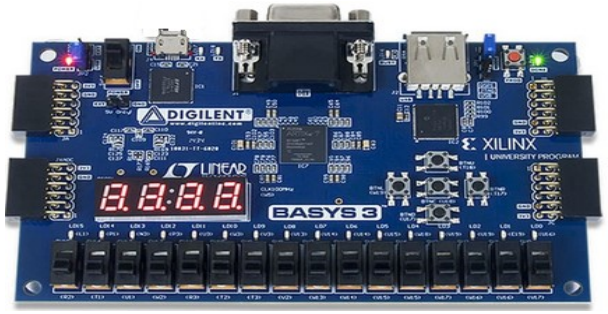


Fig. 1The BASYS 3 (FPGA) board

B. Seven- Segment Displays

Digital displays link the digital world of ones and zeros with numeric of the human world. You have seen how parallel combinations of ones and zeros can represent binary, hexadecimal, or digital numbers. For most simple instruments, digital displays use the numbers 0-9 and are represented by seven segmented displays. Each segment is controlled by a single bit, and combinations of segments turned ON or OFF can display all the numbers 0-9 and a few characters, such as A, b, c, d, E, and F. Fig. 2 shows a seven-segment display.

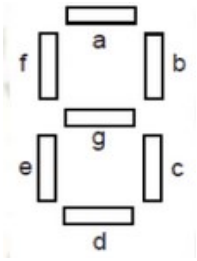


Fig. 2. Seven-Segment Display

C. PmodKYPd 16-button keypad

PmodKYPd has 16-button keypad. This keypad has 16 keys and they are arranged in an array of 4 rows and 4 columns. This keypad can be attached to one of the Pmod ports of FPGA board. On BASYS 3 we have 3 such ports, JA, JB and JC. Out of 12 pins, 8 are used for data and 4 for power supply. The PmodKYPd is shown in Fig. 3. Table 1 shows the pin out description of the PmodKYPd.

Fig. 3. PmodKYPd 16-button keypad

Table 1.Pinout description table

Header J1					
Pin	Signal	Description	Pin	Signal	Description
1	COL4	Column 4	7	ROW4	Row 4
2	COL3	Column 3	8	ROW3	Row 3
3	COL2	Column 2	9	ROW2	Row 2
4	COL1	Column 1	10	ROW1	Row 1
5	GND	Power Supply Ground	11	GND	Power Supply Ground
6	VCC	Power Supply (3.3V/5V)	12	VCC	Power Supply (3.3V/5V)

III. SIMULATION OF A CIRCUIT

In this paper, the design is based on both hardware and software. For the design to be implemented, we will be using a BASYS3 board, interface with some other hardware components.

A. Software and Simulation

Vivado 2014.4 software is used for programming and feeding in BASYS3 (FPGA) board. Vivado software is required to write the VHDL code. To run the project, PmodKYPD_7seg.vhd and PmodKYPD_7seg.xdc files are required. The VHDL files are generated with the same name as program using Vivado software.

B. Procedure of the Simulation

(1) Create a project:

a. Create a folder in C drive with the name **FPGALAB**.
b. Open Vivado and create a project in the folder location **C:\FPGALAB**.
c. Create an RTL project named FPGA_lab by selecting the following settings for BASYS-3 board.
i. Product Category – General Purpose
ii. Family – Artix-7
iii. Sub-family Artix-7
iv. Package cpg236
v. Speed -1
vi. Temp Grade C
And choose XC7A35T CPG236 -1

d. Go to project settings and make sure that default language is VHDL and project device is XC7A35T CPG236 -1

(2) Create the VHDL file

Create a VHDL design source with name PmodKYPD_7seg_BASYS.vhd and write the code.

(3) Create constraint file

Create a constraint file name PmodKYPD_7seg.xdc and save it.

(4) Simulate the file

a. Make sure that in all 3 places (Design source, constraint and simulation) PmodKYPD_7seg is the top file and set as target.
b. In constraint files make sure that only one file is enabled.
c. Go to RTL Analysis -> Open Elaborated Design -> schematic and open the schematic. It will show the schematic of our design before synthesis. Fig. 4shows RTL schematic diagram.

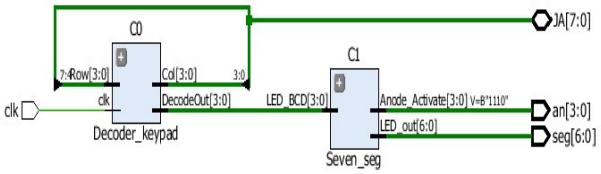
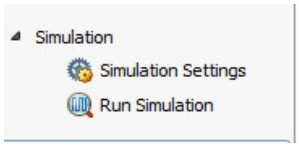
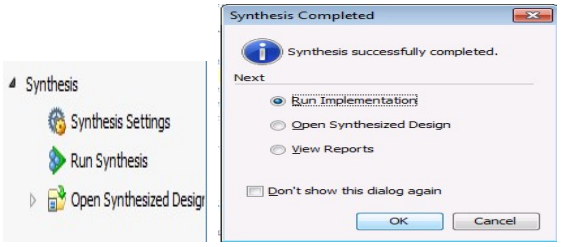


Fig. 4. RTL schematic diagram

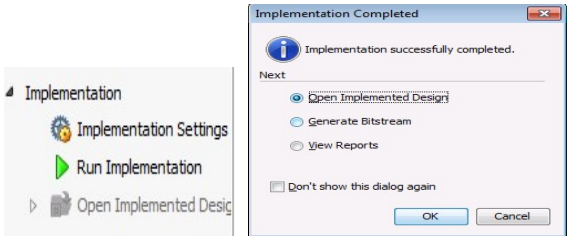
d. Go to Simulation -> Run simulation -> Run behavioral simulation.



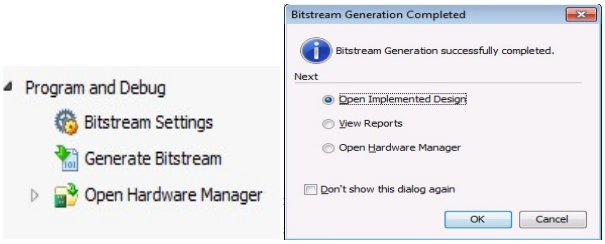
e. After successful simulation, we should synthesize our design



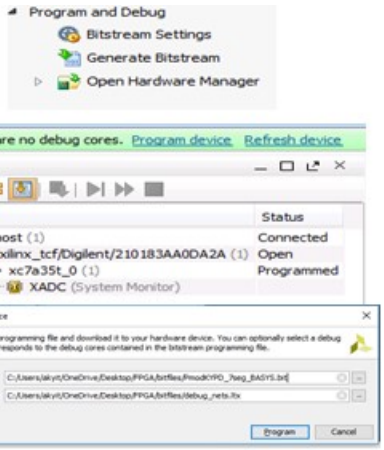
f. On successful synthesis of the design, we should implement the design.



g. After the implementation is successfully completed, we generate bitstream.



h. Select Open Hardware Manager and select program devices.



IV. HARDWARE IMPLEMENTATION

After programming the FPGA, the design is now operating on the BASYS3 board. Press the PmodKYPD (0 - 9) and (A - F). Observe how the LEDs and seven-segment displays respond to these changes. The output of a seven-segment display is shown in Fig. 5.We Press the key '1', '2' and then 'A' form the PmodKYPD, it displays the following photo.

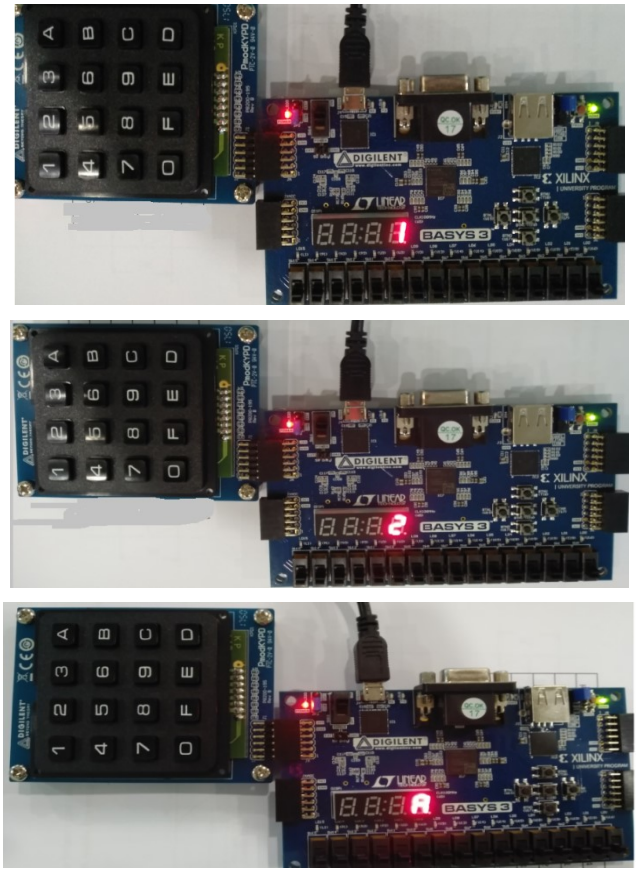


Fig. 5. Output Displays of the Circuit

V. CONCLUSIONS

The purpose of this paper is to learn how to connect simple input and output devices to an FPGA chip and implement a circuit that uses these devices. We will use the PmodKYPD 0 to 9 and A to F as inputs to the circuit. We will use one of four 7-segment displays as output devices.

ACKNOWLEDGMENT

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