International Journal of Latest Technology in Engineering, Management & Applied Science (IJLTEMAS)
Volume VIII, Issue VII, July 2019 | ISSN 2278-2540

Basics Learning for Microprocessor 8085

Khin Thet Mar[1], Khaing Khaing Wai[2], Thuzar Khin[3]
[1]*Faculty of Computer System and Technology, University of Computer Studies (Lashio), Myanmar*
[2]*Department of Information Technology Support and Maintenance, University of Computer Studies, Mandalay, Myanmar*
[3]*Faculty of Computer System and Technology, Myanmar Institute of Information Technology (MIIT), Mandalay, Myanmar*

***Abstract*— Microprocessor is an integrated circuit (IC) which incorporates core functions of a computer's central processing unit (CPU). It is a programmable multipurpose silicon chip, clock driven, register based, accepts binary data as input and provides output after processing it as per the instructions stored in the memory.**

***Keywords*— Microprocessor, Integrated circuit, Central Processing Unit**

I. INTRODUCTION

Microprocessor is a complex IC of sequential circuits. It is a programmable logic device, designed with registers, flip-flops, and timing elements. It has a set of instructions designed to manipulate data and communicate with peripherals. The process of data manipulation and communication with peripherals is determined by the logic design or the MP the logic design is called architecture.The architecture of a microprocessor is to be learnt in terms of registers, memory addressing, addressing modes, instruction set, interfacing with memory and Input and Output (I/O) devices and interrupt handling.

A. Functional Block Diagram of 8085A Microprocessor

This is the functional block diagram of the 8085 Microprocessor. It consists of various functions blocks as listed below:

1. Registers
2. Arithmetic and logic unit
3. Incrementer / Decremented address batch
4. Serial I/O control
5. Timing and control circuitry

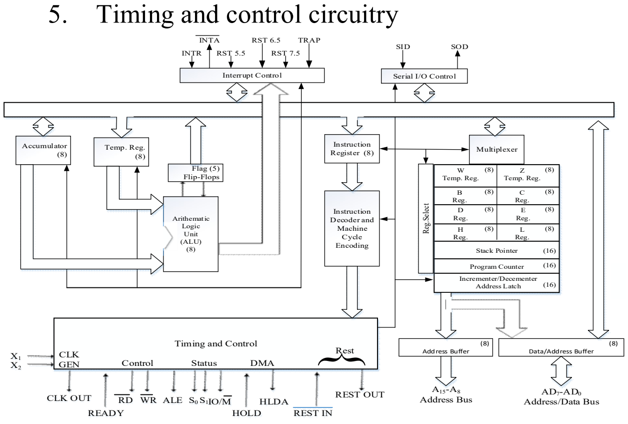

Fig. 1 The 8085 Microprocessor: Functional Block Diagram

1) Registers

It has eight addressable 8-bit registers: A, B, C, D, E, H, L, F and two 16-bit registers PC and SP. These register can be classified as :

i. General purpose registers
ii. Temporary registers (a) Temporary data register (b) W and Z registers
iii. Special purpose registers (a) Accumulator (b) Flag registers (c) Instruction register
iv. Sixteen bit registers (a) Program counter PC (b) Stack pointer (SP)

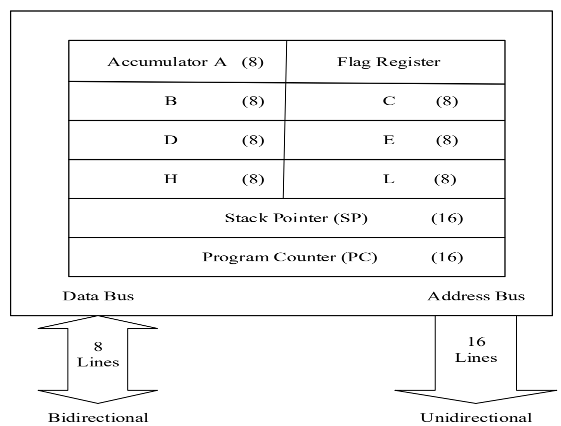

Fig. 2 The 8085 Programmable Registers

i. General Purpose Registers:

B,C,D,E,H and L are 8-bit general purpose registers can be used as a separate 8-bit registers or as 16-bit register pairs, BC,DE and HL. HL pair also functions as a data pointer or memory pointer. These are also called Scratch pad registers, as user can store data in them. To store and read data from these registers bus access is not required, it is an internal operation. Thus it provides an efficient way to store intermediate results and used them when required.

ii. Temporary Registers :

a) Temporary Data Register :

The ALU has two inputs. One input is supplied by the accumulator and other from temporarydata register. The programmer cannot access this temporary data register.

However, it isinternally used for execution of most arithmetic and logical instructions.

b) W and Z registers:

W and Z registers are temporary registers. These registers are used to hold 8-bit data duringexecution of some instruments. These registers are not available for programmer, since 8085user them internally.

iii. Special Purpose Registers:

a) Register A (Accumulator):

It is a tri-state eight bit register it is extensively used in arithmetic, logic, load and storeoperations, as well as, input / output (I/O) operations. Most of the times the result of arithmetic and logical operations is stored in the register A, hence it is also identified as accumulator.

b) Flag Register :

It is an 8-bit register, in which five of the bits carry significant information in the form of flags : S (sign flag) Z (Zero flag), AC (Auxillary carry flag)m P (Parity flag) and CY(carry flag).

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z		AC		P		CY

S-Sign flag: After the execution of arithmetic or logic operation, if bit D7 of the result is 1, the sign flag is set. In a given byte if bit D7 is 1, the number will be viewed as negative number. If D7 is 0, the number is considered as positive number.

Z-Zero flag: The zero flag sets if the result of operation in ALU is zero and flag resets if result is non zero. The zero flag is also set if a certain register content becomes zero following an increment or decrement operation of that register.

AC-Auxiliary carry flag: This flag is set if there is an overflow out of bit3 i.e., carry from lower nibble to higher nibble (D3 to D4 bit). This flag is used for BCD operations.

P-Parity flag: Parity is defined by the number of ones present in the accumulator. After an arithmetic or logic operation if the result has an even number of ones, i.e., even parity, the flag is set. If the parity is odd, flag is reset.

CY-Carry flag: This flag is set, if there is an overflow out of bit 7. The carry flag also serves as a borrow flag for subtraction.

c) Instruction register:

In a typical processor operation, the processor first fetches the opcode of instruction frommemory (i.e. it places an address on the address bus and memory responds by placing the data stored at the specified address on the data bus). The CPU stores this opcode in a register called instruction register. This opcode is further sent to the instruction decoder to select one of the alternatives.

iv. Sixteen bit registers

a) Program Counter (PC):

Program is a sequence of instructions. Microprocessor fetches these instructions from the memory and executes them sequentially. The program counter is a special purpose registerwhich, at a given time, stores the address of the next instruction to be fetched. Program counter acts as a pointer to the next instruction. How processor increments the program counter depends upon the nature of instructions: for one byte instruction it increments program counter by one, for two byte instruction it increments program counter by two and for three byte instruction it increments program counter by three such that program counter always points to the address of the next instruction.

b) Stack Pointer:

The stack is a reserved area of the memory in the RAM where temporary information may bestored. A 16-bit stack pointer is used to hold the address of the most recent stack entry.

2) Arithmetic and logic unit

The 8085's ALU performs arithmetic and logical functions on eight bit variables. The arithmetic unit performs bitwise fundamental, operation such as addition and subtraction. The logic unit performs the logical operations such as complement, AND, OR and EX-OR as well as rotate and clear. The ALU also looks after branching decisions.

3) Incrementer / Decremented address batch

This 16-bit register is used to increment or decrement the contents of program counter or stack pointer as a part of execution of instructions related to them.

Interrupt Control

The processor fetches, decodes and executes the instructions in a sequence. Sometimes it isnecessary to have the processor automatically execute one of a collection of special routineswhenever special condition exists within a program or the microcomputer system. After theexecution of special routine, the program control must be transferred to the program whichprocessor was executing before the occurrence of the special condition. The occurrence of this special condition is referred as interrupt. The interrupt control block has five interrupt inputs RST 5.5, RST 6.5, RST 7.5, TRAP and INTR and one acknowledge signal INTA.

4) Serial I/O Control

In situations like, data transmission over long distance and communication with cassette tapes or CRT terminal, it is necessary to transmit data bit by bit to reduce the cost of cabling. In serial communication one bit is transferred at a time over a single line. The 8085's serial I/O control provides two lines, SID and SOD for serial communication. The Serial Output Data (SOD) line is used to send data serially and Serial Input Data (SID) line is used to receive data serially.

5) Timing and control circuitry

There are three control signals and status signals. ALE, RD and WR are control signals and S_0, S_1 and IO/M are status signals. It controls all external and internal circuits.

B. Bus Structure of 8085 Microprocessor

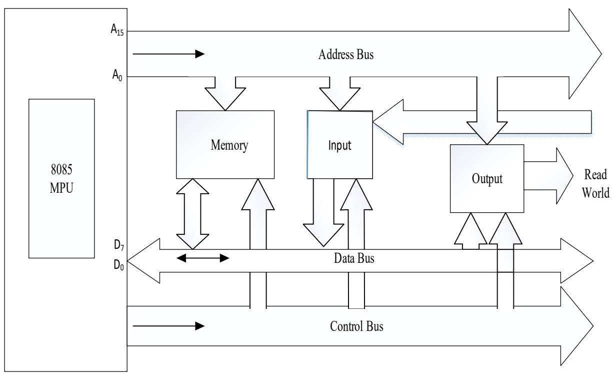

Fig. 3The 8085 Bus Structure

1. Address Bus:-The address bus is a group of 16 lines generally identified as A0 to A15. the address bus is unidirectional: bits flow in one direction – from the MPU to peripheral devices. The MPU uses the address bus to perform the first function: identifying a peripheral or a memory location. In a computer system, each peripheral or memory location is identified by a binary number called an address and the address bus is used to carry a 16-bit address. This is similar to postal address of a house.We can find that how much memory location it can use the formula 2^ N. where

N is the number of bits used for address lines.

2. Data Bus:- The data bus is a group of eight lines used for data flow. These lines are bidirectional – data flow in both directions between the MPU and memory and peripheral devices. The MPU uses the data bus to perform the second function: transferring binaryinformation. The eight data lines enable the MPU to manipulate 8- bit data ranging from 00 to FF.

3. Control Bus:-The control bus is comprised of various signal lines that carry synchronization signals. The MPU uses such lines to perform the third function: provide timing signals. The control signals are not group of lines like address or data buses, but individual lines that provide pulse to indicate an MPU operation. The MPU generates specific control signals for every operation (such as memory read or I/O write) it performs. These signals are used to identify a device type with which the MPU intends to communicate.

C. Pin Diagram and Pin description of 8085

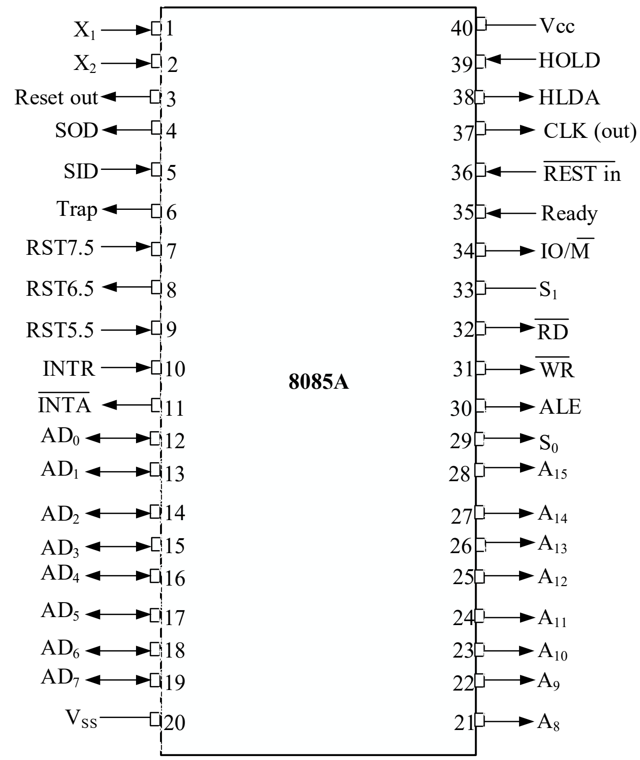

Fig. 4 The 8085 Microprocessor Pinout

1. Power Supply and Clock Frequency

The power supply and frequency signals are as follows:

Vcc: +5V power supply.**Vss:** Ground reference.

X1, X2: A crystal is connected at these two pins. The frequency is internally dividedby two; therefore, to operate a system at 3MHz and, the crystal should have frequencyof 6MHz.

CLK (OUT) — Clock out: This signal is used as the system clock for other devices.

2. Address Bus

The 8085 has eight lines, A15-A8,which are nidirectional and used as the high order address bus.

3. Multiplexed Address / Data Bus

The signal lines AD7-AD0 are bidirectional: they serve a dual purpose. They are used as the low order address bus as well as the data bus. In executing an instruction, during the earlier part of the cycle, these lines are used as the low-order address bus. During the later part of the cycle, these lines are used as the data bus. (This is also known as multiplexing the bus.) However, the low-order address bus can be separated from these signals by using a latch.

4. Control and Status Signals

This group of signals includes two control signals (RD and WR), three status signals (IO/M, S1, and S0) to identify the nature of the operation, and one special signal (ALE) to indicate the beginning of the operation. These signals are as follows:

ALE — Address Latch Enable: This is positive going pulse generatedevery time the 8085 begins an operation (machine cycle); it indicates that the bits onAD7-AD0 are address bits. This is used primarily to latch the low-order address from themultiplexed bus and generate a separate set of eight address lines, A7-A0.

$\overline{RD}$— *Read:* This read control signal (active low). This signal indicates that theselected I/O or memory device is to be read and data are available on the data bus.

$\overline{WR}$ — Write: This is a write control signal (active low). This signal indicates thatthe data on the data bus are to be written on into a selected memory device or I/Olocation.

IO/$\overline{M}$: This is status signal used to differentiate between I/O and memoryoperations. When it is high, it indicates an I/O operation; when it is low, it indicates amemory operation. This signal combines with RD and WR to generate I/O and memory control signals.

S1 and S0: These status signals, similar to IO/M, can identify various operations, butthey are rarely used in small systems.

TABLE I

8085 Machine Cycle Status and Controls Signals

IO/M	S_1	S_0	Control Signals	OPERATION
0	1	1	$\overline{RD}$=0	Opcode fetch
0	1	0	$\overline{RD}$=0	Memory read
0	0	1	$\overline{WR}=0$	Memory write
1	1	0	$\overline{RD}$=0	I/O read
1	0	1	$\overline{WR}=0$	I/O write
1	1	1	$\overline{\text{INTA}}=0$	Interrupt acknowledge
z	0	0	$\overline{RD},\overline{WR} = z\ and\ \overline{\text{INTA}}=1$	Halt
z	x	x		Hold
z	x	x		Rest

Externally Initiated Signals, Including Interrupts

The 8085 has five interrupt signals that can be used to interrupt a program execution. The interrupt signals are Interrupt Request (INTR), Restart Interrupts (RST5.5, RST 6.5, RST7.5) and TRAP. The microprocessor acknowledges an interrupt request by the INTA (Interruptacknowledge) signal. In addition to the interrupts, three pins — RESET, HOLD, and READY— accept the externally initiated signals as inputs. To respond to the HOLD request, the 8085has one signal called HLDA (Hold Acknowledge).

INTR(input)	Interrupt Request: This is used as a general-purpose interrupt.
INTA(Output)	Interrupt Acknowledge: This is used to acknowledge an interrupt.
RST 7.5(inputs) RST 6.5 RST 5.5	Restart Interrupts: These are vectored interrupts and transfer the program control to specific memory locations. They have higher priorities than the INTR interrupt. Among these three, the priority order is 7.5, 6.5 and 5.5
TRAP(input)	This is a non maskable interrupt and has the highest priority
HOLD(input)	This signal indicates that a peripheral such as a DMA controller is requesting the use of the address and data buses.
HLDA	Hold Acknowledge: This signal acknowledges the HOLD request.
READY	. This signal is used to delay the microprocessor Read or Write cycles until a slow-responding peripheral is ready to send or accept data. When this signal goes low, the microprocessor waits for an integral number of clock cycles until it goes high.

RESET, HOLD and READY are additional interrupts. They accept the externally initiated signals as inputs. To respond to the HOLD request, it has one signal called HLDA.

RESET IN: When the signal on this pin goes low, the program counter is set to zero, the buses are tri-stated, and the microprocessor is reset.

RESET OUT: This signal indicates that the microprocessor is being reset. The signal can be used to reset other devices.

SERIAL I/O PORTS

The microprocessor has 2 pins specially designed for software –controlled serial I/O. one is called SOD (Serial Output Data) and the other is called SID (Serial Input Data). Data transfer is controlled through 2 instructions: SIM and RIM. The instruction SIM is necessary to output data serially from the SOD line. Similarly instruction RIM is used to input serial data through the SID line.

The SID and SOD lines in the 8085 eliminate the need for an input port and an outputport in the software-controlled serial I/O. Essentially, the SID is a 1-bit port and SOD is a 1-bit output port.

D. THE 8085 INSTRUCTION SET

The 8085 instructions can be classified into the following five functional categories:

1. Data transfer (copy) operations
2. Arithmetic operations
3. logical operations
4. Branching operations and
5. Machine control operations.

1. Data Transfer (Copy) Operations

a. **Load** a 8-bit number 4F in register B	**MVI B, 4FH**
b. **Copy** from Register B to Register A	**MOV A,B**
c. **Load** a 16-bit number 2050 in Register pair HL	**LXI H, 2050H**
d. **Copy** from Register B to Memory Address 2050	**MOV M,B**
e. **Copy** between Input/Output Port and Accumulator	**OUT 01H** **IN 07H**

2. Arithmetic Operations

Add a 8-bit number 32H to Accumulator	**ADI 32H**
Add contents of Register B to Accumulator	**ADD B**
Subtract a 8-bit number 32H from Accumulator	**SUI 32H**
Subtract contents of Register C from Accumulator	**SUB C**
Increment the contents of Register D by 1	**INR D**
Decrement the contents of Register E by 1	**DCR E**

3. Logical & Bit Manipulation operations

Logically AND Register H with accumulator	**ANA H**
Logically OR Register L with Accumulator	**ORA L**
Logically XOR Register B with Accumulator	**XRA B**
Compare contents of Register C with Accumulator	**CMP C**
Complement Accumulator	**CMA**
Rotate Accumulator Left	**RAL**

4. Branching Operations

These operations are used to control the flow of program execution

Jump to a 16-bit Address 2080H if **C**arry flag is **SET**	**JC 2080H**
Unconditional **Jump**	**JMP 2050H**
Call a subroutine with its 16-bit Address	**CALL 3050H**
Return back from the Call	**RET**
Call a subroutine with its 16-bit Address if **C**arry flag is **RESET**	**CNC 3050H**
Return if **Z**ero flag is **SET**	**RZ**

5. Machine Control Instructions

These instructions affect the operation of the processor. For e.g.

HLT	Stop program execution
NOP	Do not perform any operation

E. Programming model

The processor has seven 8-bit registers accessible to the programmer, named A, B, C, D, E, H, and L, where A is also known as the accumulator. The other six registers can be used as independent byte-registers or as three 16-bit register pairs, BC, DE, and HL, depending on the particular instruction. Some instructions use HL as a 16-bit accumulator. As in the 8080, the contents of the memory address pointed to by HL can be accessed as pseudo register M. It also has a 16-bit program counter and a 16-bit stack pointer to memory. Instructions such as PUSH PSW, POP PSW affect the Program Status Word. The accumulator stores the results of arithmetic and logical operations, and the flags register bits are set or cleared according to the results of these operations. The sign flag is set if the result has a negative sign. The auxiliary or half carry flag is set if a carry- over from bit 3 to bit 4 occurred. The parity flag is set according to the parity of the accumulator. The zero flag is set if the result of the operation was 0. Lastly, the carry flag is set if a carry-over from bit 7 of the accumulator occurred.

F. Application

The microprocessor is provided with an instruction set consisting of various instructions such as MOV, ADD, SUB, JMP, etc. These instructions are written in the form of a program which is used to perform various operations such as branching, addition, subtraction, bitwise logical, and bit shift operations. More complex operations and other arithmetic operations must be implemented in software. For example, multiplication is implemented using a multiplication algorithm.

REFERENCES

[1]. Microprocessor architecture programming and applications with the 8085
[2]. https://www.geeksforgeeks.org/bus-organization-of-8085-microprocessor/
[3]. http://www.codebind.com/microprocessor/pin-diagram-pin-description-8085-microprocessor/
[4]. https://www.geeksforgeeks.org/interrupts-8085-microprocessor/
[5]. https://newhorizonindia.edu/nhc_kasturinagar/wp-content/uploads/2018/10/Unit-2-Microprocessor.pdf
[6]. https://archive.codeplex.com/?p=8085simulator