Design of Multiplexers, Decoder and a Full Subtractor using Reversible Gates

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***Abstract*- This paper shows an effective design of combinational circuits such as 2:1, 4:1 multiplexers, 2:4 decoder and a full subtractor using reversible gates. This paper also evaluates number of reversible gates used and garbage outputs in implementing each combinational circuit.**

***Keywords* - Reversible Logic Gates, Multiplexer, Decoder, Full Subtractor Garbage output**

I. INTRODUCTION

In the early 1960, R. Landauer proved that irreversible computation results in KTln2 joules of energy dissipation due to the each bit of information loss where K = Boltzmann's constant, T = Temperature at which computation is performed [1]. Later in 1973, C.H. Bennett showed that KTln2 joules of energy dissipation can be eliminated, if the computation is performed in a reversible manner [2].

A multiplexer or MUX is a device that selects between different analog or digital input signals and forwards it to a single output signal. A MUX of 2^n inputs has n select lines, which are used to select which input line is to be sent to the output. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines [3]. A full Subtractor is a combinational circuit that performs subtraction of two bits, one is minuend and other is subtrahend. The full subtractor circuit has three inputs and two outputs. The three inputs A, B and Bin, denote the minuend, subtrahend and previous borrow respectively. The two outputs D and Bout represent the difference and output borrows respectively.

II. REVERSIBLE LOGIC

'Reversible Computation' is defined as a model of computation where computational process at some extent, is reversible. It means that it can reserve the data as long as it requires and when needed [4]. Reversible gate is basically an n X n logic gate, where, if 'n' inputs are given, we will get 'n' outputs. Properties of reversible logic are like it can recover the state of inputs from the outputs, it follows bijective mapping i.e. when 'n' number of inputs are taken, and one can get 'n' number of outputs from the gates. The circuit obtained will be acyclic, i.e. feedback will be there but Fan-out will not be more than one. Parameters to determine the complexity and performance of circuits[5,6] are the number of reversible gates, garbage output which is the number of unused outputs used in the reversible gates, and quantum cost which is the cost of the circuit with respect to the cost of a primitive gate.In the past few decades, the Reversible logic has emerged as one of the promising research areas find its applications in various emerging technologies such as Bioinformatics, Cryptography, Optical computing, Nanotechnology, DNA computing, and Quantum computing etc [7].

III. REVERSIBLE GATES USED

There are several number of reversible gates used to implement various complex circuits, but in this paper, we have used 3X3 NFT GATE to implement multiplexers (both 2:1 and 4:1), 3X3 TOFFOLI GATE to implement 2:4 Decoder and three reversible gates (4X4 HNG GATE, 2X2 FEYNMANN GATE, 3X3 FREDKIN GATE) to implement a full subtractor using two half subtractors.

1. *NFT Gate:*

It is a 3X3 gate with inputs A, B and C and outputs X, Y and Z, where X = A XOR B, Y = B'C XOR AC, Z = BC XOR AC'.

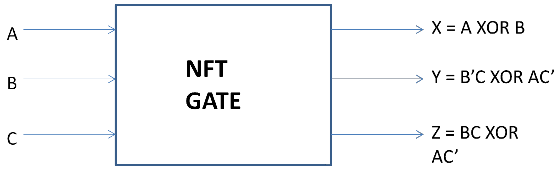

Fig.1 denotes the basic logic diagram of NFT Gate

2. *TOFFOLI Gate:*

It is a 3X3 reversible gate with inputs A, B and C and outputs X, Y and Z, where X = A,

Y = B, Z = (A.B) XOR C [8].

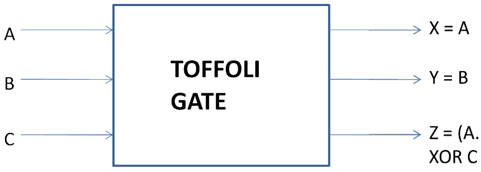

Fig. 2 denotes the basic logic diagram of TOFFOLI Gate

3. HNG Gate:

It is a 4X4 reversible gate with inputs A, B, C and D and outputs W, X, Y and Z, where W= A, X = B, Y = A XOR B XOR C XOR D, Z = (A XOR B).C XOR (A.B) XOR D.

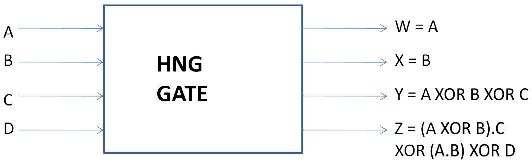

Fig. 3 denotes the basic logic diagram of HNG Gate.

4. FEYNMANN Gate:

It is a 2x2 reversible gate with inputs A and B and outputs X and Y, where X = A and Y = A XOR B.

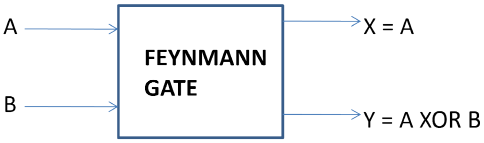

Fig. 4 denotes the basic logic diagram of FEYNMANN Gate.

5. FREDKIN Gate:

It is a 3X3 reversible gate with inputs A, B and C and outputs X, Y and Z, where X = A, Y = (A'.B) XOR (A.C), Z = (A'.C) XOR (A.B).

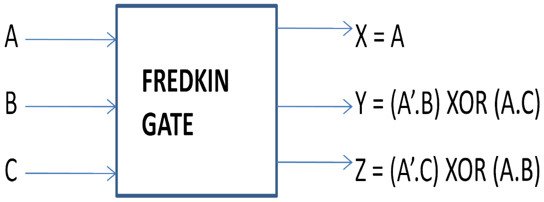

Fig. 5 denotes the basic logic diagram of FREDKIN Gate

IV. MULTIPLEXER

Multiplexer or 'MUX' is a combinational logic circuit, which is designed for switching of several input lines to a single common output line by the application of a control signal. MUX can be of different forms like 2:1, 4:1, 8:1, and 16:1 and many more. That means, if 2^n input lines are given, one can get one output line in case of a multiplexer.

The basic logic diagram and truth table of a 2:1 MUX is shown in Fig. 6(A) and 6(B) respectively.

A. 2:1 MUX:

For a 2:1 MUX, the output line (Y) is given by:

$$Y = S.I1 + S'.I0 \qquad (1)$$

Where, I0 and I1 are the input lines, S is the select line and Y is the output line.

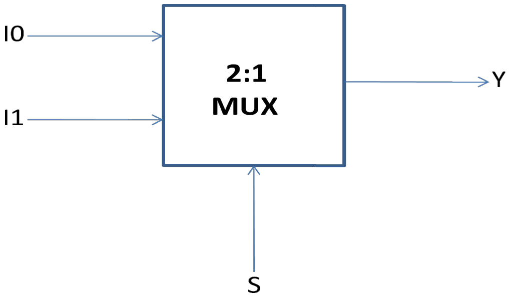

Fig. 6(A)

S	I0	I1	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Fig. 6(B)

Fig.6: (A) denotes the basic logic diagram of 2:1 MUX, where S is the select line, I0 and I1 are the input lines and Y is the output line. (B) denotes the truth table of the same.

B. 4:1 MUX:

The basic logic diagram and truth table of a 4:1 MUX is shown in Fig. 7(A) and 7(B) respectively.

For a 4:1 MUX, the output line (Y) is given by:

$$Y = S0'.S1'.I0 + S0.S1'.I1 + S0'.S1.I2 + S0.S1.I3 \qquad (2)$$

Where, I0, I1, I2 and I3 are input lines, S0 and S1 are select lines and Y is the output line.

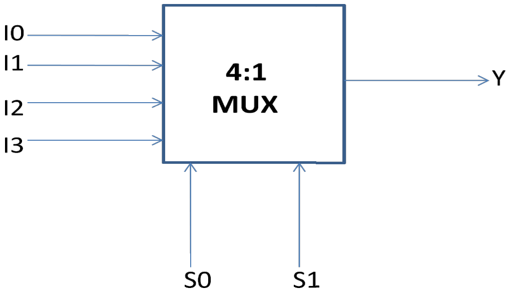

Fig. 7(A)

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Fig. 7(B)

Fig.7: (A) denotes the basic logic diagram of 4:1 MUX, where S0, S1 are the select lines, I0 to I3 are the input lines and Y is the output line. (B) denotes the truth table of the same.

C. *Multiplexers Using Reversible Gates:*

For implementing 2:1 MUX, one 3X3 NFT gate is required and for implementing 4:1 MUX, three 3X3 NFT gates are required.

The implementation of 2:1 and 4:1 multiplexers is shown in Fig.8 and 9 respectively.

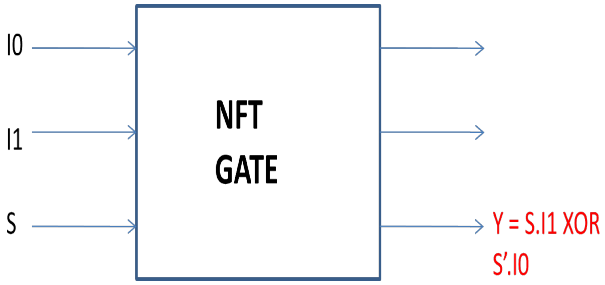

Fig. 8 denotes the implementation of 2:1 MUX using 3X3 NFT Gate, where I0, I1 and S are the input lines and Y is the output line.

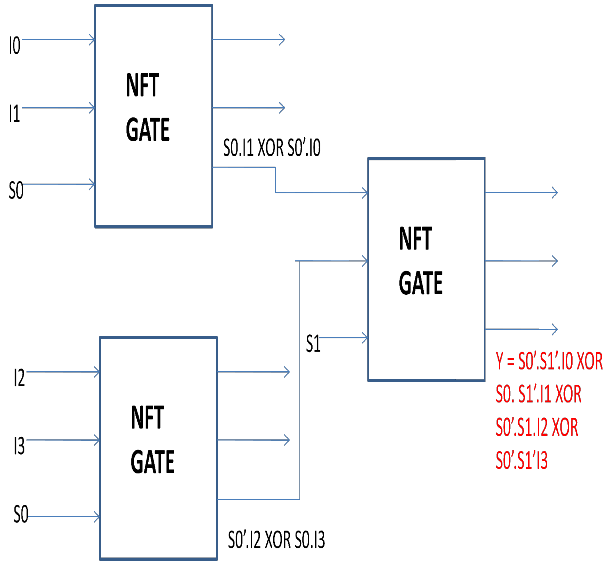

Fig. 8 shows the implementation of 4:1 MUX using three 3X3 NFT Gates, where I0 to I3 and S0, S1 are input lines and Y is the output line.

V. DECODER

A Decoder is a combinational circuit which changes a code into a set of signals. It has 'n' inputs and 2^n outputs. Decoders are simpler to design. Suppose, the numbers of inputs are 8, then the number of outputs will be 2^8 or 256.

Let us take an example of a 2:4 Decoder using reversible gates.

A. *2:4 Decoder:*

In a 2:4 decoder, there are four output lines, such as,

$$I0 = A.B \qquad (3)$$

$$I1 = A'.B \qquad (4)$$

$$I2 = A.B' \qquad (5)$$

$$I3 = A'.B' \qquad (6)$$

Where, A and B are the input lines and I0 to I3 are the output lines.

The basic block diagram and truth table of a 2:4 Decoder is shown in Fig. 9(A) and (B) respectively.

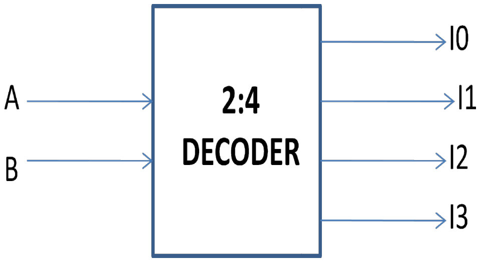

Fig. 9(A)

E	A	B	I0	I1	I2	I3
0	×	×	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Fig. 9(B)

Fig.9: (A) denotes the basic logic diagram of 2:4 Decoder, where A and B are the input lines and I0 to I3 are the output lines and (B) denotes the truth table of the same.

B. *2:4 Decoder Using Reversible Gates:*

2:4 decoder can be implemented using four 3X3 TOFFOLI gates and two 1X1 NOT gates. The diagram is shown in Fig. 10.

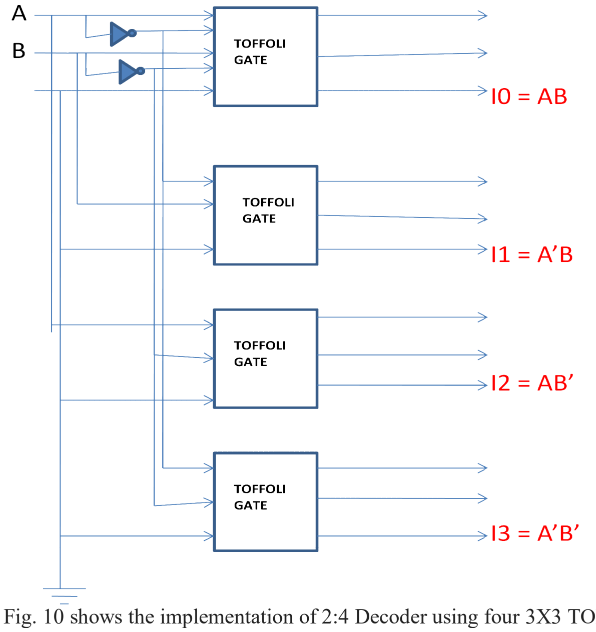

Fig. 10 shows the implementation of 2:4 Decoder using four 3X3 TOFFOLI Gates and two 1X1 NOT gates, where A, B are the input lines and I0, I1, I2 and I3 are the output lines.

VI. FULL SUBTRACTOR

A subtractor can be designed like an adder using same approach. A full subtractor is a combinational circuit, used to perform subtraction of three inputs, the minuend, the subtrahend and borrow in. Two output lines are generated which are difference and borrow out. A reversible half subtractor is designed using two TSG gates in [4]. A full subtractor can be designed using two half subtractors. Difference output and borrow out output can be given as:

$$Difference = A\ XOR\ B\ XOR\ Bin \qquad (7)$$

$$Borrow\ out = (A\ XOR\ B)'.Bin\ XOR\ (A'.B) \qquad (8)$$

Where, A, B and Bin are the inputs and Difference and Borrow out are the outputs.

The block diagram and truth table of a Full Subtractor is shown in Fig. 11(A) and (B) respectively.

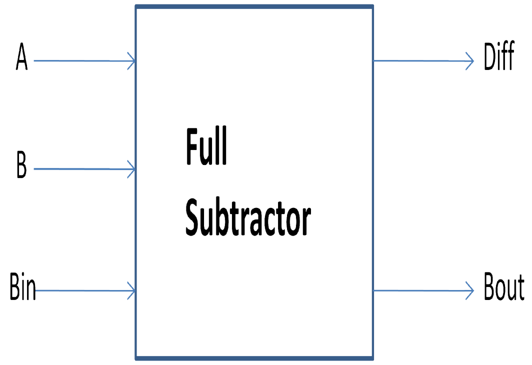

Fig. 11(A)

A	B	Bin	Diff	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Fig. 11(B)

Fig.11: (A) denotes the basic block diagram of Full Subtractor, where A, B, and Bin are the input lines, and Diff denotes difference output line, and Bout denotes the borrow out output line. (B) denotes the truth table of the same.

B. Full Subtractor Using Reversible Gates:

A full subtractor circuit can be implemented using three reversible gates, such as 4X4 HNG gate, 2X2 FEYNMANN gate and 3X3 FREDKIN gate in Fig.12.

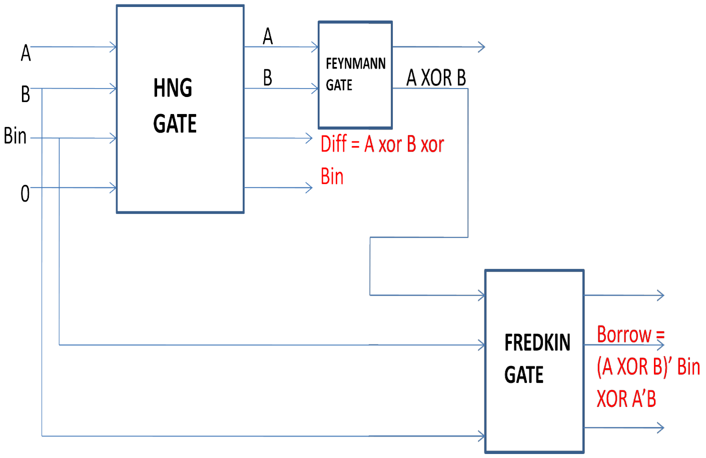

Fig. 12 shows the implementation of Full Subtractor using reversible gates, where A, B and Bin are the input lines and Diff denotes the Difference output line and Borrow denotes the borrow output line.

VII. PERFORMANCE ANALYSIS

METHODS	GARBAGE OUTPUTS	NO. OF REVERSIBLE GATES
2:1 MUX	2	1
4:1 MUX	8	3
2:4 DECODER	8	6
FULL SUBTRACTOR	4	3

Fig. 13 shows the performance details of number of gates, garbage outputs of the above implementations.

The table of Fig. 13 shows the performance of the implemented device using reversible gates in terms of number of gates and the garbage outputs.

VIII. CONCLUSION

In this paper, 2:1 and 4:1 multiplexers, 2:4 decoder and a full subtractor has been implemented using reversible gates in an efficient way. For the designing of 2:1 and 4:1 multiplexers, numbers of gates used are 1 and 3. Garbage outputs are 2 and 8 respectively. For the designing of 2:4 decoder, the number of gates used and garbage outputs are 6 and 8 respectively and in case of a full subtractor, number of gates used are 3 and garbage outputs are 4. So, one can implement these combinational circuits using these reversible gates from the details shown in the table.

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